NSI6601M-Q1

Single-Channel Isolated Gate Driver

Datasheet (EN) 1.1

Product Overview

The NSI6601M is a family of high reliability single-channel isolated gate driver ICs which can be designed to drive IGBTs, power MOSFETs and SiC MOSFETs in many applications. That provide minimum peak output currents up to 5A and an integrated active Miller Clamp circuit with the same current rating .

The NSI6601M provides 3000Vrms isolation in SOP8 package, and 5700Vrms isolation in SOW8 package. System robustness is supported by 150kV/μs minimum common-mode transient immunity (CMTI).

The driver operates with a maximum supply voltage of 28V, while the input-side accepts from 3V to 17V supply voltage. Under voltage lock-out (UVLO) protection is supported by all the power supply voltage pins.

Because of high driving current ability, excellent robustness, wide supply voltage range and fast signal propagation, NSI6601M is suitable for high reliability, power density and efficient switching power system.

Key Features

- Isolated single-channel driver
- Active Miller Clamp
- Input side supply voltage: 3V to 17V
- Driver side supply voltage: up to 28V with 9V, and 12V UVLO options
- 5A peak source and sink output current
- Minimum CMTI: ±150kV/μs
- 80ns typical propagation delay
- RoHS & REACH Compliance
- Operation temperature: -40°C ~125°C
- AEC-Q100 Grade1

Safety Regulatory Approvals

- UL recognition:
  - SOW8: 5700V_{rms} for 1 minute per UL1577
  - SOP8: 3000V_{rms} for 1 minute per UL1577
- DIN VDE V 0884-11:2017-01
- CSA component notice 5A
- CQC certification per GB4943.1-2011

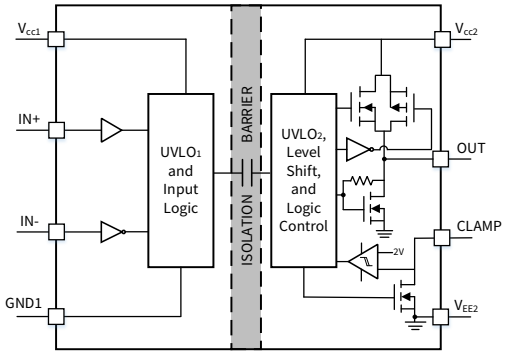
Applications

- Isolated DC/DC and AC/DC Power Supplies
- High Voltage PFC
- Solar Inverters
- Motor Drives and EV Charging
- UPS and Battery Chargers

Device Information

Part Number	*UVLO Level*	*Package*	*Body Size*
NSI6601MB-Q1SWVR	9V	SOW8	7.5×5.85×2.3mm
NSI6601MC-Q1SWVR	12V	SOW8	7.5×5.85×2.3mm
NSI6601MB-Q1SPR	9V	SOP8	4.9×3.9×1.35mm
NSI6601MC-Q1SPR	12V	SOP8	4.9×3.9×1.35mm
NSI6601WC-Q1SWVR	12V	SOW8	7.5×5.85×2.3mm

Block Diagram



NSI6601M/W Diagram

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1. Pin Configuration and Function

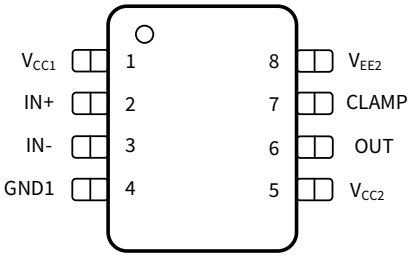


Figure 1.1NSI6601MC/MB
(Top View)

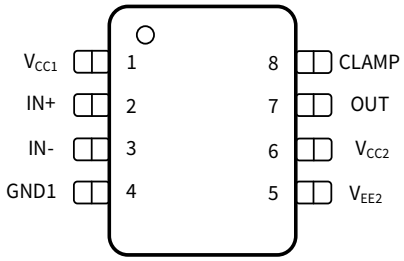


Figure 1.2 NSI6601WC
(Top View)

Table 1.1 NSI6601M/W Pin Configuration and Description

PIN NAME	PIN NO.		TYPE	FUNCTION
	NSI6601MC/B	NSI6601WC		
V_{CC1}	1	1	P	Input-side supply rail
IN+	2	2	I	Non-inverted input signal with internal pull down to GND1
IN-	3	3	I	Inverted input signal with internal pull up to VCC1
GND1	4	4	G	Input-side ground reference
V_{CC2}	5	6	P	Positive output supply rail
OUT	6	7	O	Gate Driver Output
CLAMP	7	8	I	Active Miller-Clamp input
V_{EE2}	8	5	G	Driver-side ground reference

2. Absolute Maximum Ratings

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	V_{CC1}-GND1	-0.3	18	V
Input Signal Voltage	V_{IN+}-GND1, V_{IN-}-GND1	-0.3	18	V
Driver Side Supply Voltage	V_{CC2}-V_{EE2}	-0.3	35	V
Output Signal Voltage	V_{OUT} - V_{EE2}, V_{CLAMP}- V_{EE2}	V_{EE2}-0.3	V_{CC2}+0.3	V
Junction Temperature	T_J	-40	150	°C
Storage Temperature	T_{stg}	-65	150	°C

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	Human body model (HBM), per AEC-Q100-002-RevD ● All pins	±4000	V
	Charged device model (CDM), per AEC-Q100-011-RevB ● All pins	±1500	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Input Side Supply Voltage	V_{CC1}-GND1	3	17	V
Input Signal Voltage	V_{IN+}-GND1, V_{IN-}-GND1	-0.3	17	V
Driver Side Supply Voltage	V_{CC2}-V_{EE2} (NSI6601MB)	10	28	V
	V_{CC2}-V_{EE2} (NSI6601MC)	13	28	
Ambient Temperature	T_A	-40	125	°C

5. Thermal Information

Parameters	Symbol	SOW8	SOP8	Unit
Junction–to-ambient thermal resistance(1)	R_{JA}	110	120	°C/W
Junction-to-case(top) thermal resistance2)	$R_{JC(top)}$	45	60	°C/W
Junction–to-top characterization parameter(3)	Ψ_{JT}	18	38	°C/W

Junction-to-board characterization parameter[3)]	Ψ_{JB}	47	59	°C/W

1)Standard JESD51-3 Low Effective Thermal Conductivity Test Board (2s2p) in an environment described in JESD51-2a.

2)Standard JESD51-3 Low Effective Thermal Conductivity Test Board (1s) by transient dual interface test method described in JESD51-14.

3)Obtained by Simulating in an environment described in JESD51-2a.

6. Specifications

6.1. DC Electrical Characteristics

V_{CC1}=5V, with a bypass capacitor of 1μF from V_{CC1} to GND1, and V_{CC2}=15V with a capacitor of 10μF from V_{CC2} to V_{EE2} , Ta=-40℃ to 125℃, Unless otherwise noted, Typical values are at Ta=25℃.

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Condition*
Supply Currents						
Input Supply Quiescent Current	I_{CC1}		0.9	1.5	mA	V_{IN+}= GND1, V_{IN-}=5V
Output Supply Quiescent Current	I_{CC2}		1.6	3	mA	V_{IN+}= GND1, V_{IN-}=GND1
Input Side Supply UVLO Threshold						
VCC1 UVLO Rising Threshold	V_{CC1_ON}		2.9	3.1	V	
VCC1 UVLO Falling Threshold	V_{CC1_OFF}	2.55	2.78		V	
VCC1 UVLO Hysteresis	V_{CC1_HYS}		0.12		V	
Driver Side Supply UVLO Threshold (NSI6601MB 9V UVLO Level)						
VCC2 UVLO Rising Threshold	V_{CC2_ON}		9.2	10	V	
VCC2 UVLO Falling Threshold	V_{CC2_OFF}	8	8.5		V	
VCC2 UVLO Hysteresis	V_{CC2_HYS}		0.7		V	
Driver Side Supply UVLO Threshold (NSI6601MC,NSI6601WC 12V UVLO Level)						
VCC UVLO Rising Threshold	V_{CC2_ON}		12.2	13	V	
VCC UVLO Falling Threshold	V_{CC2_OFF}	10.3	11.2		V	
VCC UVLO Hysteresis	V_{CC2_HYS}		1		V	
Input Pin Characteristics						
Logic High Input Threshold (IN+, IN-)	V_{IN+H}, V_{IN-H}		0.55×V_{CC1}	0.7×V_{CC1}	V	
Logic Low Input Threshold (IN+, IN-)	V_{IN+L}, V_{IN-L}	0.3×V_{CC1}	0.45×V_{CC1}		V	
Input Hysteresis Voltage (IN+, IN-)	V_{IN_hys}		0.1×V_{CC1}		V	
IN+ Input Current	I_{IN+}		55	70	μA	V_{IN+}= V_{CC1}
IN- Input Current	I_{IN-}	-70	-55		μA	V_{IN-}=GND1
Output Pin Characteristics						
High Level Output Voltage (V_{CC2}-V_{OUT})	V_{OH}		140	320	mV	I_{OUT}=-50mA, V_{IN+}=High, V_{IN-}=Low
Low Level Output Voltage (OUT)	V_{OL}		30	70	mV	I_{CLAMP}=50mA,V_{IN+}=Low, V_{IN-}=High

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Output Pull-up Resistance	R_{OH}		2.8		Ω	V_{OH}/50mA
Output Pull-down Resistance	R_{OL}		0.6		Ω	V_{OL}/50mA
Peak Source Current	I_{OH}		5		A	V_{IN+}=High, V_{IN-}=Low, pulse width<10μs
Peak Sink Current	I_{OL}		5		A	V_{IN+}=Low, V_{IN-}=High, pulse width<10μs
Active Miller Clamp						
Clamp Low Level Voltage	V_{LL_CLAMP}		11.2	24	mV	I_{CLAMP}=20mA,V_{IN-}=V_{IN+}=Low
Clamp Threshold Voltage	V_{CLAMP_TH}		2.1	2.3	V	Referred to V_{EE2}
Low Level Clamp Current (Peak)	I_{LL_CLAMP}		5		A	V_{IN-}=V_{IN+}=Low, V_{CLAMP}=2V pulse
Clamp Delay Falling	T_{CD}		46		ns	
Short Circuit Clamping						
Clamping Voltage (OUT) (V_{OUT} - V_{CC2})	V_{CLP_OUT}		1	1.6	V	I_{OUT}=500mA with t_{pulse}=10μs, V_{IN+}=High, V_{IN-}=Low
Clamping Voltage (CLAMP) (V_{CLAMP}-V_{CC2})	V_{CLP_CLAMP}		1.2	1.5	V	I_{CLAMP}=500mA with t_{pulse}=10μs, V_{IN+}=High, V_{IN-}=Low
			0.7	1	V	I_{CLAMP}=20mA, V_{IN+}=High, V_{IN-}=Low
Active Pull-down						
Active Pull-down Voltage on CLAMP (V_{CLAMP} to V_{EE2})	V_{ACTPD}		2.3		V	I_{CLAMP}=0.1*$I_{CLAMP(typ)}$, V_{CC1}= V_{CC2}=Open

6.2. Switching Characteristics

Switching characteristics are measured by using V_{CC1}=5V, 1μF capacitor from V_{CC1} to GND1, and V_{CC2}=15V with 10μF bypass capacitor from V_{CC2} to V_{EE2}, Ta=-40℃ to 125℃, Unless otherwise noted, Typical values are at Ta=25℃.

Parameter	*Symbol*	*Min*	*Typ*	*Max*	*Unit*	*Condition*
Minimum Pulse Width	t_{PWmin}		30	60	ns	
Propagation Delay	t_{pLH}	50	80	110	ns	C_{LOAD}=100pF
Propagation Delay	t_{pHL}	50	80	110	ns	C_{LOAD}=100pF
Pulse Width Distortion $\|t_{PLH}-t_{PHL}\|$	t_{PWD}		2	25	ns	C_{LOAD}=100pF
Output Rise Time (20% to 80%)	t_R		9	20	ns	C_{LOAD}=1nF
Output Fall Time (80% to 20%)	t_F		8	18	ns	C_{LOAD}=1nF
Common Mode Transient Immunity[1)]	CMTI	150			kV/μs	verified by design

6.3. Typical Performance Characteristics

Typical characteristics are measured by using V_{CC1}=5V, 1μF capacitor from V_{CC1} to GND1, and V_{CC2}=15V with 10μF bypass capacitor from V_{CC2} to V_{EE2} T_J =-40°C to 125°C (unless otherwise noted).

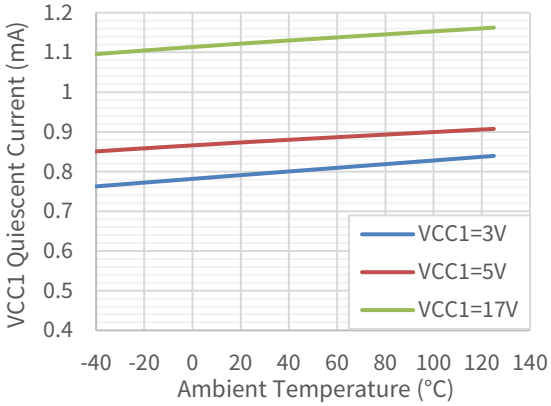


Figure 6.1 Input supply quiescent current Vs Temperature

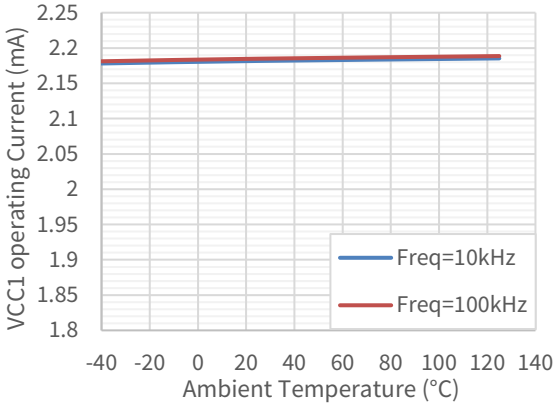


Figure 6.2 Input supply operating current Vs Temperature

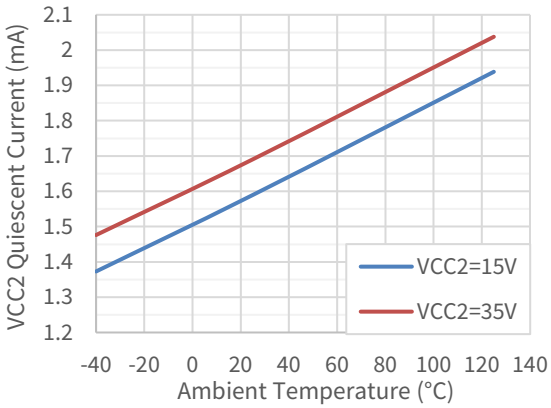


Figure 6.3 Output supply quiescent current Vs Temperature

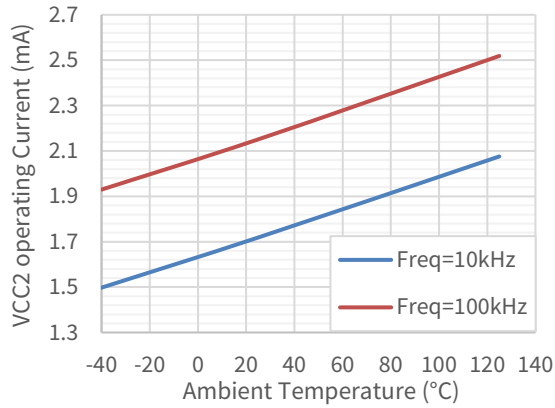


Figure 6.4 Output supply operating current Vs Temperature

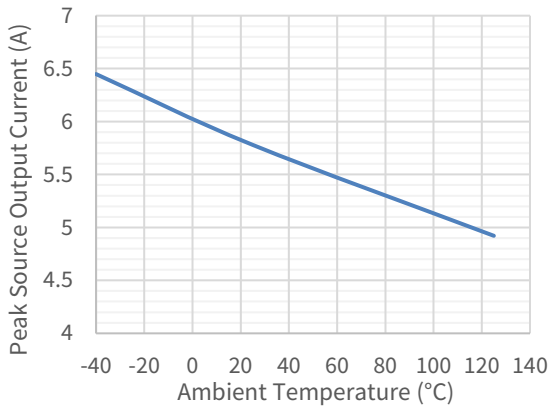


Figure 6.5 Peak source output current Vs Temperature

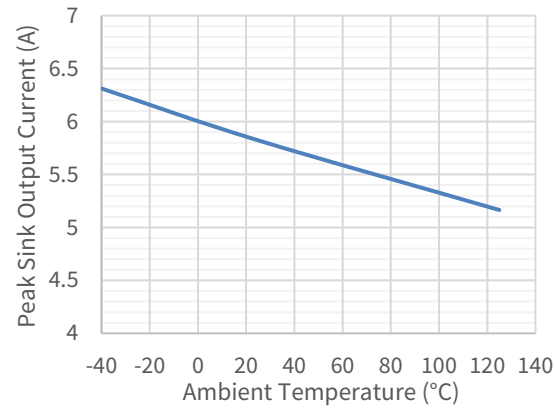


Figure 6.6 Peak sink output current Vs Temperature

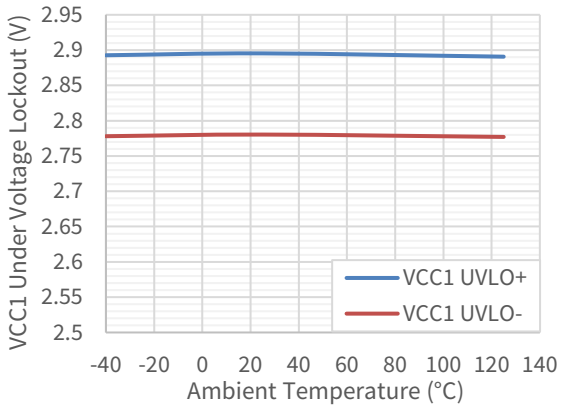


Figure 6.7 VCC1 UVLO Threshold Vs Temperature

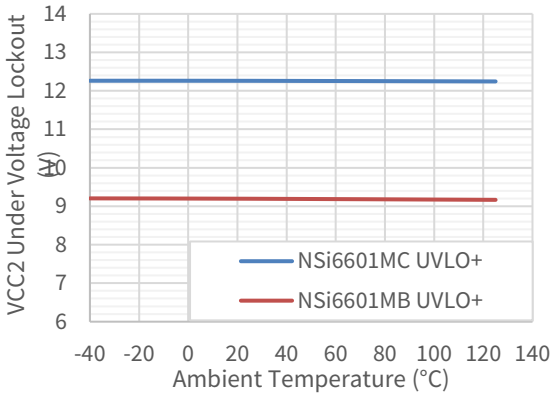


Figure 6.8 VCC2 UVLO_ON Vs Temperature

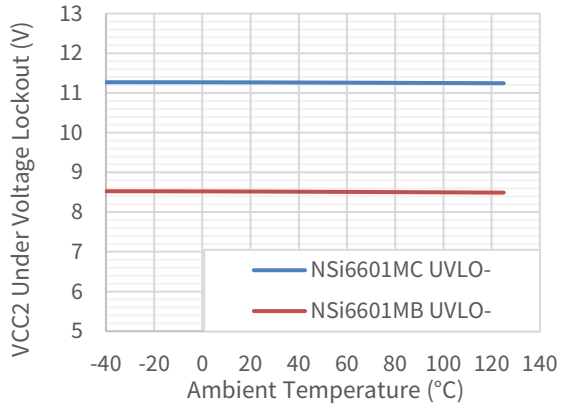


Figure 6.9 VCC2 UVLO_OFF Vs Temperature

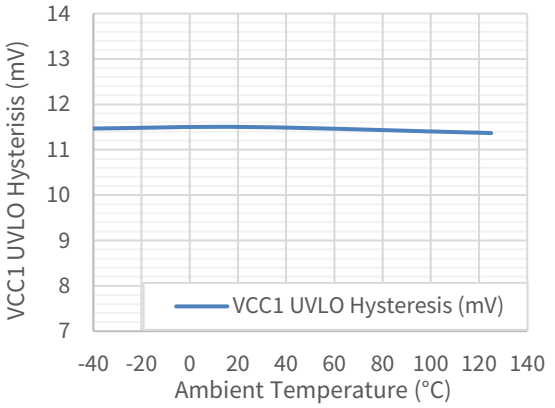


Figure 6.10 VCC1 UVLO Hysteresis Vs Temperature

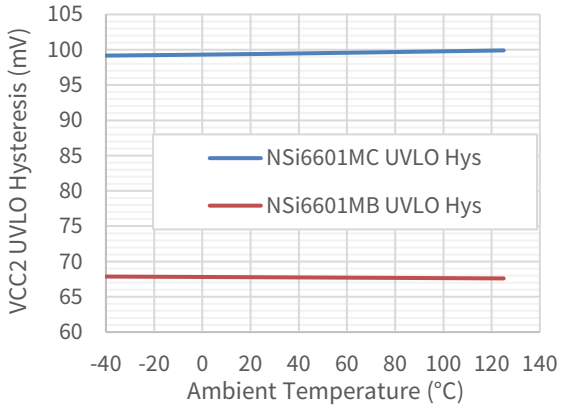


Figure 6.11 VCC2 UVLO Hysteresis Vs Temperature

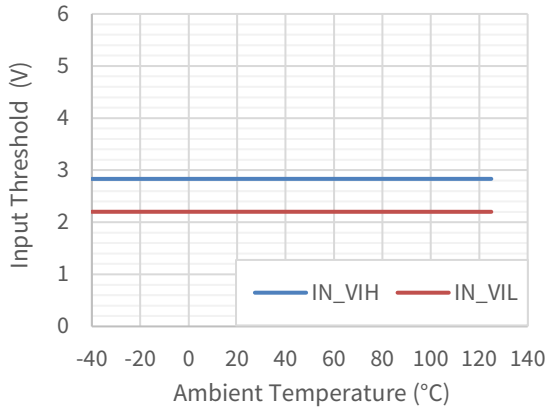


Figure 6.12 Input Threshold Vs Temperature

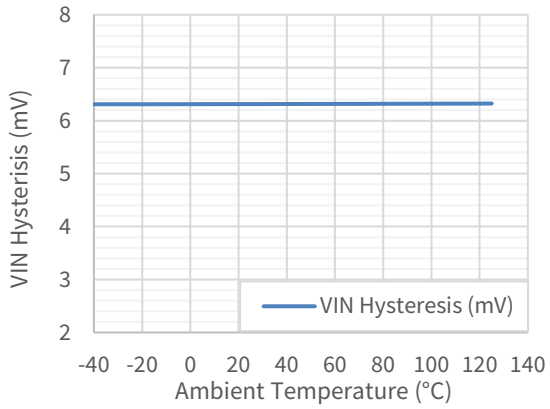


Figure 6.13 Input Hysteresis Vs Temperature

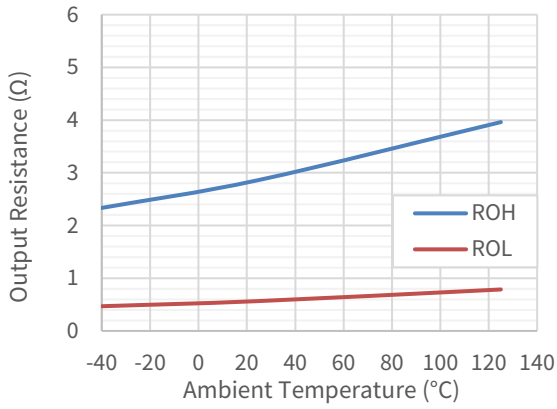


Figure 6.14 Output Resistance Vs Temperature

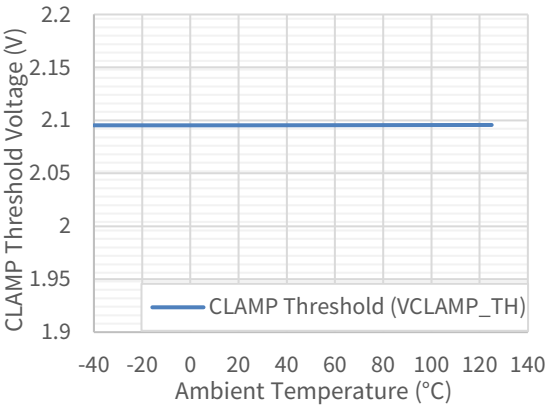


Figure 6.15 CLAMP Threshold Voltage Vs Temperature

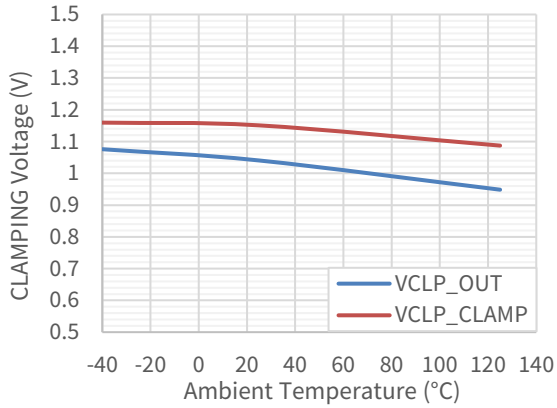


Figure 6.16 CLAMPING Voltage Vs Temperature

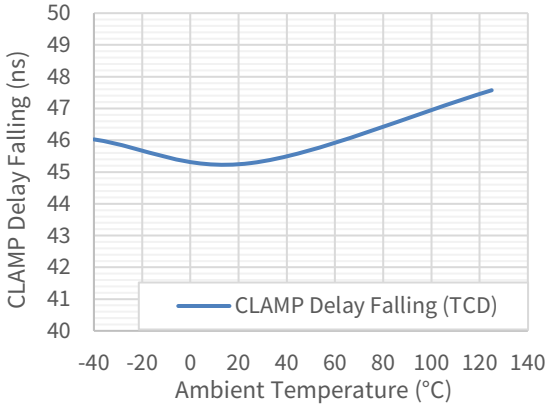


Figure 6.17 CLAMP Delay Falling Vs Temperature

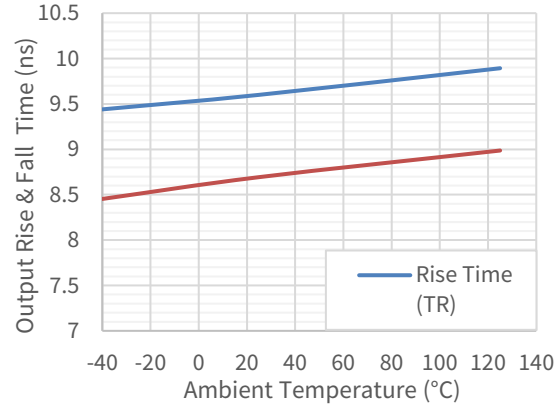


Figure 6.18 Output rise and fall time Vs Temperature

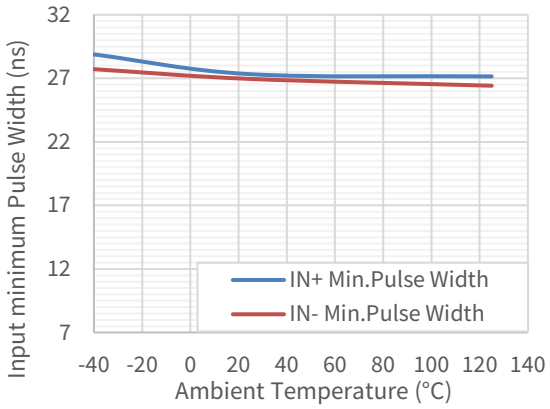


Figure 6.19 Minimum Pulse Width Vs Temperature

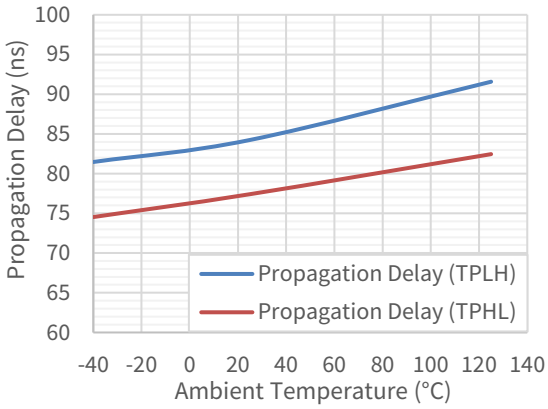


Figure 6.20 Propagation Delay Vs Temperature

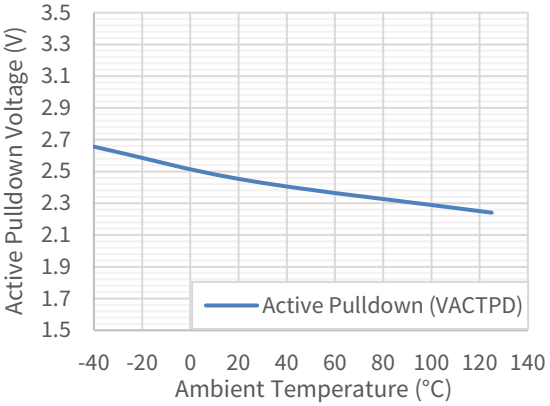


Figure 6.21 Active Pull-down Voltage Vs Temperature

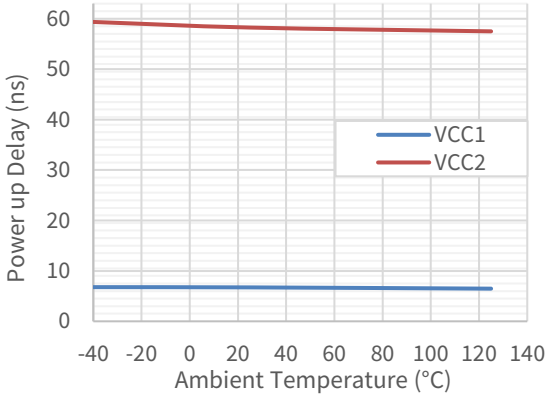


Figure 6.22 Power up Delay Vs Temperature

6.4. Parameter Measurement Information

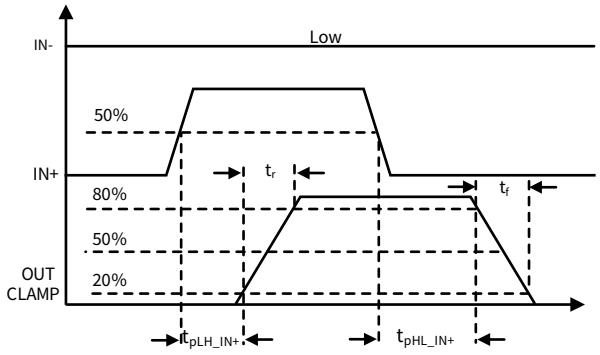


Figure 6.23 Propagation Delay, Rise Time and Fall Time (For Non-Inverting Configuration)

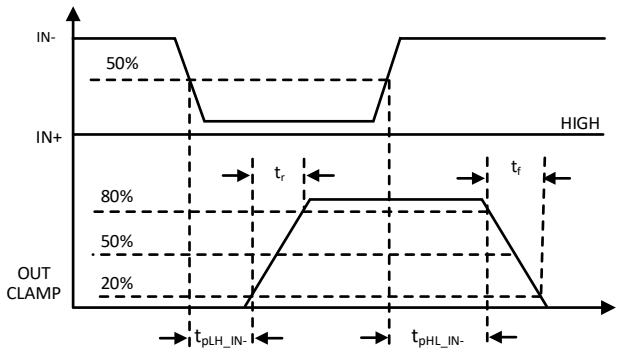


Figure 6.24 Propagation Delay, Rise Time and Fall Time (For Inverting Configuration)

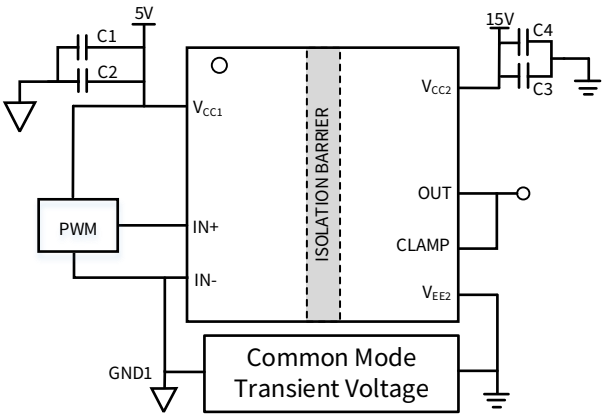


Figure 6.25 Common-Mode Transient Immunity Test Circuit

7. High Voltage Feature Description

7.1. Insulation Characteristics

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
			SOW8	SOP8	
Min. External Air Gap (Clearance)		CLR	8	4	mm
Min. External Tracking (Creepage)		CPG	8	4	mm
Distance through the Insulation		DTI	20		μm
Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	CTI	>600		V
Material Group	IEC 60664-1		I		
Overvoltage Category per IEC60664-1	For Rated Mains Voltage ≤ 150Vrms		I to IV	I to IV	
	For Rated Mains Voltage ≤ 300Vrms		I to IV	I to III	
	For Rated Mains Voltage ≤ 600Vrms		I to IV	I to II	
	For Rated Mains Voltage ≤ 1000Vrms		I to III	/	
Climatic Category			40/125/21		
Pollution Degree			2		
DIN EN IEC 60747-17(VDE 0884-17)					
Maximum Working Isolation Voltage	AC voltage	V_{IOWM}	1500	700	V_{RMS}
	DC voltage		2121	990	V_{DC}
Maximum Repetitive Isolation Voltage		V_{IORM}	2121	990	V_{peak}
Apparent Charge	Input to Output Test Voltage, Method B1, $V_{pd(m)}=V_{IORM}\times1.5$, 100% production test, $t_{ini}=t_m=1s$	q_{pd}	/	<5	pC
	Method A , After Environmental Tests Subgroup 1,$V_{pd(m)}=V_{IORM}\times1.2$, $t_{ini}=60s$, $t_m=10s$		/		pC
	After Input and Output Safety Test Subgroup 2 and Subgroup 3,$V_{pd(m)}=V_{IORM}\times1.2$,$t_{ini}=60s$, $t_m=10s$		/		pC
Apparent Charge	Method B1,$V_{pd(m)}=V_{IORM}\times1.875$, 100% production test, $t_{ini}=t_m=1s$	q_{pd}	<5	/	pC
	Method A , After Environmental Tests Subgroup 1,$V_{pd(m)}=V_{IORM}\times1.6$, $t_{ini}=60s$, $t_m=10s$			/	pC

Description	Test Condition	Symbol	Value		Unit
	Method A , After Input and Output Safety Test Subgroup 2 and Subgroup 3,$V_{pd(m)}$=V_{IORM}×1.2, t_{ini}=60s, t_m=10s, partial discharge <5pC			/	pC
Maximum Transient Isolation Voltage	t = 60 sec	V_{IOTM}	8000	4242	V_{peak}
Maximum impulse voltage	Tested in air, 1.2/50μs waveform per IEC62368-1	V_{imp}	6000	3500	V
Maximum Surge Isolation Voltage	Test method per IEC62368-1, 1.2/50μs waveform, VIOSM≥VIMP × 1.3	V_{IOSM}	10000	6000	V_{peak}
Isolation Resistance	V_{IO} =500V at T_A=T_S=25°C	R_{IO}	>10^{12}		Ω
	V_{IO} = 500 V, T_{amb} = T_S		>10^{9}		Ω
	V_{IO} = 500 V, 100 °C ≤ T_{amb} ≤ 125 °C		>10^{11}		Ω
Isolation Capacitance	f = 1MHz	C_{IO}	0.6		pF
UL1577					
Insulation voltage per UL	V_{TEST} = V_{ISO}, t = 60s (qualification),V_{TEST} = 1.2×V_{ISO},t = 1s(100% production test)	V_{ISO}	5700	3000	V_{rms}

7.2. Safety Limiting Values

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI6601xx-Q1SWVR

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
Maximum Safety Temperature		T_S	150		°C
Maximum Safety Power Dissipation	$R_{\theta JA}$=110°C/W, T_J=150°C, T_A=25°C	P_S	Total	1.04	W
			Input Side	0.05	
			Output Side	0.99	
Maximum Safety Current	$R_{\theta JA}$=110°C/W, V_{CC2}=15V, T_J=150°C, T_A=25°C	I_S	Output Side	73	mA
	$R_{\theta JA}$=110°C/W, V_{CC2}=30V, T_J=150°C, T_A=25°C		Output Side	36	

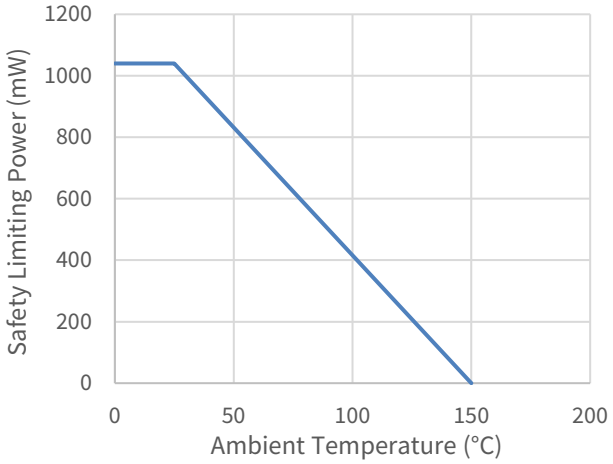


Figure 7.1 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-11 for SOP8 Package

Reinforced isolation safety-limiting values as outlined in VDE-0884-17 of NSI6601xx-Q1SPR

Description	*Test Condition*	*Symbol*	*Value*		*Unit*
Maximum Safety Temperature		T_S	150		°C
Maximum Safety Power Dissipation	$R_{\theta JA}$=120°C/W, T_J=150°C, T_A=25°C	P_S	Total	1.14	W
			Input Side	0.05	
			Output Side	1.09	
Maximum Safety Current	$R_{\theta JA}$=120°C/W, V_{CC2}=15V, T_J=150°C, T_A=25°C	I_S	Output Side	66	mA
	$R_{\theta JA}$=120°C/W, V_{CC2}=30V, T_J=150°C, T_A=25°C		Output Side	33	

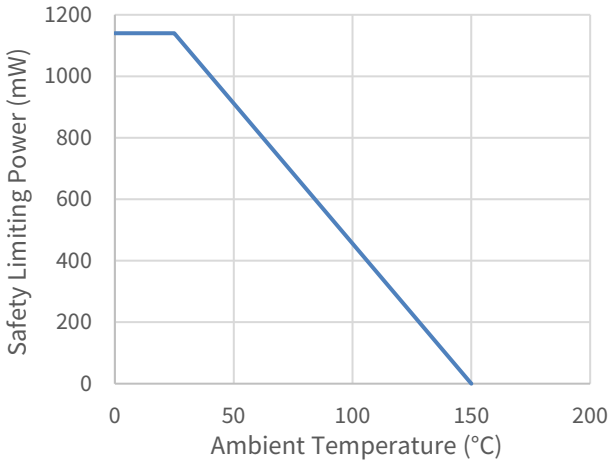


Figure 7.4 Thermal Derating Curve for Limiting Power per DIN VDE V 0884-17 for SOW8 Package

7.3. Safety-Related Certifications

The NSI6601M-Q1SWVR are approved or pending approval by the organizations listed in table.

UL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022
Single Protection, 5700V_{RMS} Isolation Voltage	Single Protection, 5700V_{RMS} Isolation voltage	Reinforced Insulation V_{IORM}=2121V_{PEAK}, V_{IOTM}=8000V_{PEAK}, V_{IOSM}=10000V_{PEAK}	Reinforced Insulation
Certificate No.E500602		Certificate No.40050121	CQC20001264940

The NSI6601M-Q1SPR are approved or pending approval by the organizations listed in table.

UL		*VDE*	*CQC*
UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to GB4943.1-2022
Single Protection, 3000V_{RMS} Isolation Voltage	Single Protection, 3000V_{RMS} Isolation voltage	Basic Insulation V_{IORM}=990V_{PEAK}, V_{IOTM}=4242V_{PEAK}, V_{IOSM}=6000V_{PEAK}	Basic Insulation
Certificate No.E500602		Certificate No.40050121	CQC20001264940

8. Function Description

8.1. Overview

The NSI6601M is a highly reliable isolated gate driver with 9V, and 12V UVLO versions, which is suitable to drive MOSFET, IGBT, and SiC. The NSI6601M is available in SOP8 narrow body and wide body package, which can support 3000VRMS or 5700VRMS isolation per UL1577. System robustness is supported by 150kV/μs minimum common-mode transient immunity (CMTI).

The functional block diagram of NSI6601M is shown in Figure 8.1. Two Input pins with non-inverting and inverting logic support interlock and shoot through protection. Low resistance of high side and low side MOSFET in the output stage ensures high driving capability. Split outputs help to control the rise and fall time individually. Active miller clamping and short circuit clamping features are implemented to protect power transistor.

The isolation barrier inside NSI6601M is based on a capacitive isolation. The signal across the isolation barrier transmit through OOK (on-off keying) modulation technique with key benefits of high noise immunity and low radiation EMI. The transmitter sends a high-frequency carrier across the isolation barrier to represent one digital state and sends no signal to represent the other digital state. As shown in Figure 8.2, the digital signal is modulated with RF carrier generated by the internal oscillator at the transmitter side, then it is transferred through the capacitive isolation barrier and demodulated at the receiver side.

8.2. Functional Block Diagram

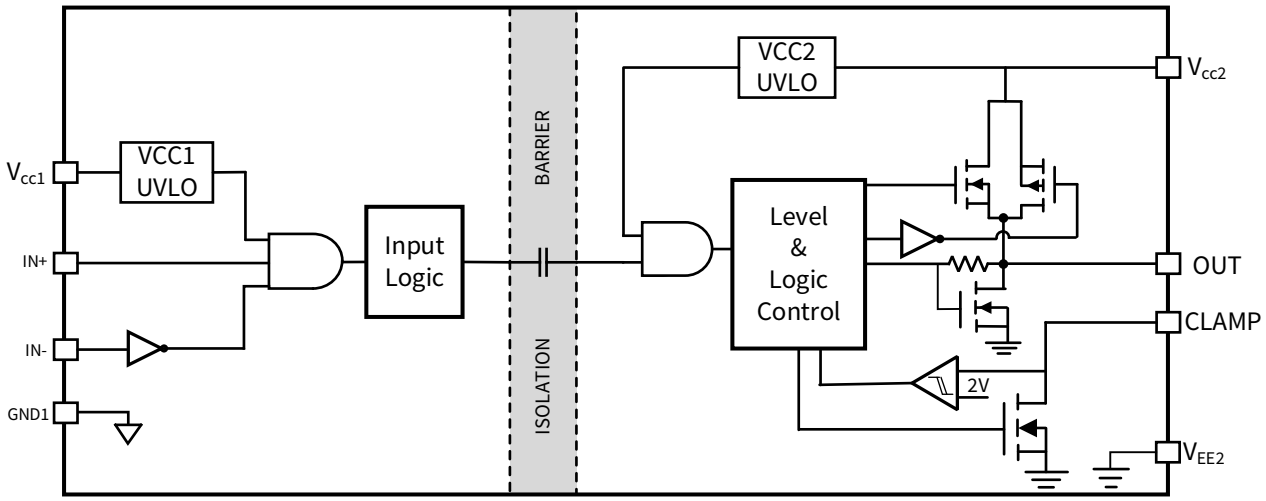


Figure 8.1 NSI6601MB/MC Functional Block Diagram

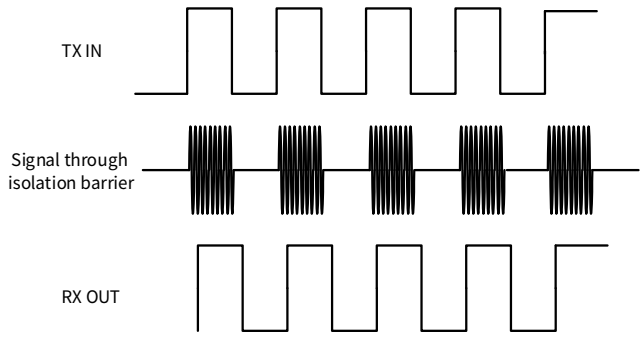


Figure 8.2 OOK based Modulation

8.3. Truth Tables

Table 8.1 Driver Function Table (1)

V_{CC1} status	V_{CC2} status	Inputs			Comment
		IN+	IN-	OUT	
PU	PU	H	L	H	
PU	PU	L	H	L	
PU	PU	H	H	L	Interlock protection
PU	PU	L	L	L	
PD	PU	X	X	L	
PU	PD	X	X	L	Active pull-down
PD	PD	X	X	L	Active pull-down

(1) PD = Powered Down; PU = Powered Up; H = Logic High; L= Logic Low; X= Irrelevant

The IN+ pin is internally pulled down to GND1, while IN- pin is internally pulled up to VCC1, making the output of NSI6601 is low by default. To improve noise immunity, grounding an input or tying to VCC1 is recommended.

8.4. Output Stage

The voltage and current of external power transistor drain to source or collector to emitter change during low to high output signal transition. At that moment, the N-channel MOSFET turns-ON to pull up OUT more quickly to provide a transitory boost in the sourcing current during the period of turning the output state from low to high. It results external power transistor faster turn on time, lower turn on power loss, also leads to smaller temperature increase of NSI6601M. The equivalent pull-up resistance of NSI6601M is the parallel combination of R_{OH} || R_{NMOS}. This equivalent resistance results a very small value, indicating the strong driving capability of NSI6601M. The pull-down resistance R_{OL} of N-channel MOSFET is also very small. That also indicates the strong driving capability of NSI6601M. Since the P-channel MOSFET only conducts during the dc measurement while the N-channel MOSFET remain OFF for this interval. So the R_{OH} parameter is associated with the on-resistance of P-channel MOSFET in dc measurements.

Typical values of pull-up and pull-down internal resistance are listed in table 8.2.

Table 8.2 NSI6601M Output Stage On-Resistance

R_{NMOS}	R_{OH}	R_{OL}	R_{CLAMP}	Unit
0.8	2.8	0.6	0.6	Ω

In miller-clamp output configuration as shown in Figure 8.3, the pull-down structure works as two parallel N-channel MOSFETs structure when the CLAMP and OUT pins connect to the gate of the IGBT or MOSFET.

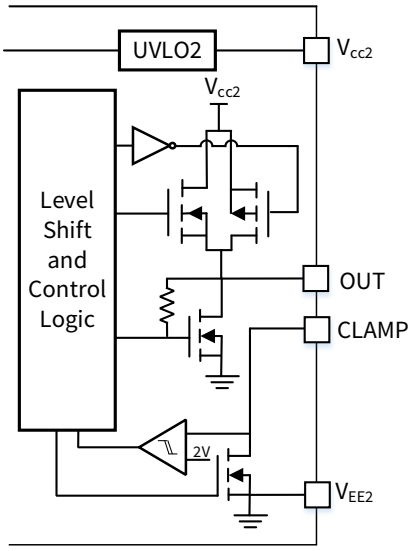


Figure 8.3 NSI6601M Output Stage

8.5. V_{CC1}, and V_{CC2} Under Voltage Lock Out (UVLO)

The NSI6601M has an internal under voltage lock out (UVLO) protection on both input and output side source blocks. The driver output is held low by an active clamp circuit when the supply voltage of VCC1 or VCC2 is lower than VCC_ON at power-up status or lower than VDD_OFF after power-up, regardless of the status of the input pins.

The VCC1_GND1 and VCC2_VEE2 ULVO protections have hysteresis (VCC1_HYS & VCC2_HYS) to prevent chatter noise from VCC supply and allow small drops in supply power which are usually happened in start up. It also prevents sags in the VCC, cause by sudden increase in ICC current while system commences switching.

8.6. Active Pull-Down

This function helps to pull the IGBT or MOSFET gate to the off-state when VCC2 is not connected to the power supply. This feature prevents the false turn-on of OUT and CLAMP pins by clamping the output to approximately 2V.

8.7. Short Circuit Clamping

Short circuit is used to clamp the driver output voltage as well as to pull the miller clamp pins to a bit higher than VCC2. This function helps to protect the gate of a MOSFET or IGBT from over-voltage breakdown. The short circuit clamping is implemented by adding an additional circuit between the dedicated pins and the VCC2. The internal diode circuitry can conduct 500mA current to the supply for 10us.Use of external schottky diode may be added to improve the current capability and tighter clamping.

8.8. Active Miller Clamp

The active miller clamp function helps to prevent the false turn-on of the power switches caused by the miller current in applications such as half bridge configuration. Where switched off IGBT turns to dynamically turn-on during turn on period of the opposite IGBT. It usually happens when a uni-polar power supply is used. To avoid such false turn-on of switches a miller clamp allows sinking the miller current across a low impedance path in this dv/dt situation. During turn-off the gate voltage is monitored and the power-switch gate voltage is clamped to less than 2V referred to VEE2. The clamp is designed for a miller current in the same range as the nominal output current.

9. Application Note

9.1. Typical Application Circuit

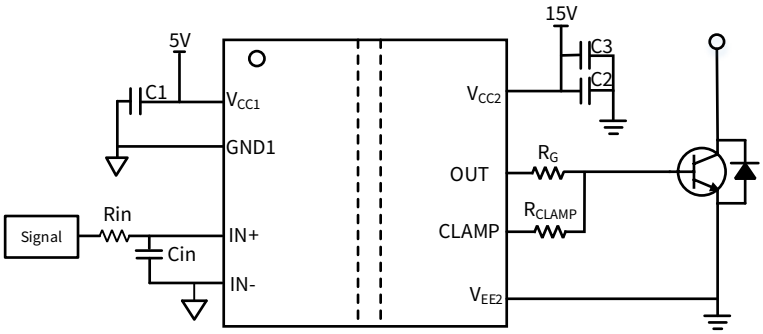


Figure 9.1 NSI6601M Typical Application Circuit

Bypassing capacitors for V_{CC1} and V_{CC2} supplies are needed to achieve reliable performance. To filter noise, 0.1μF/50V ceramic capacitor is recommended to place as close as possible to NSI6601M, both at V_{CC1} and V_{CC2} side. For V_{CC2} supply, additional 10μF/50V ceramic capacitor is recommended, to support high peak currents when turning on external power transistor. If the V_{CC1} or V_{CC2} power supply is located long distance from the IC, bigger capacitance is needed.

The input filter composed by Rin and Cin can be used if input PWM has ring due to long traces or bad PCB layout. However, it will introduce longer propagation delay.

9.2. Interlock Protection

For applications to drive power transistors in half bridge configuration, two NSI6601M can be used. Interlock protection is possible as shown in Figure 9.2. If the controller has some mistake, leading to negative dead time, the output PWM of NSI6601M is adjusted to avoid power transistor shoot through.

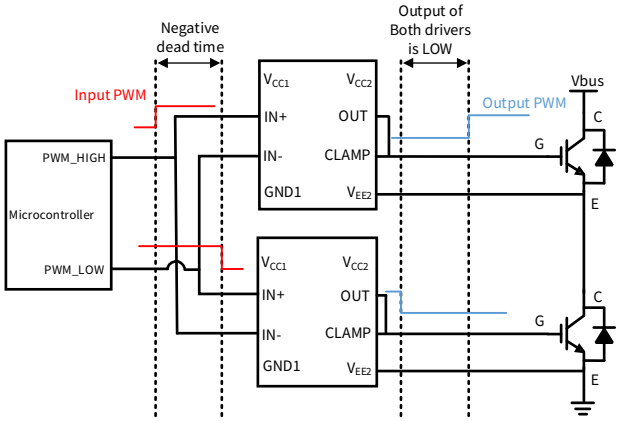


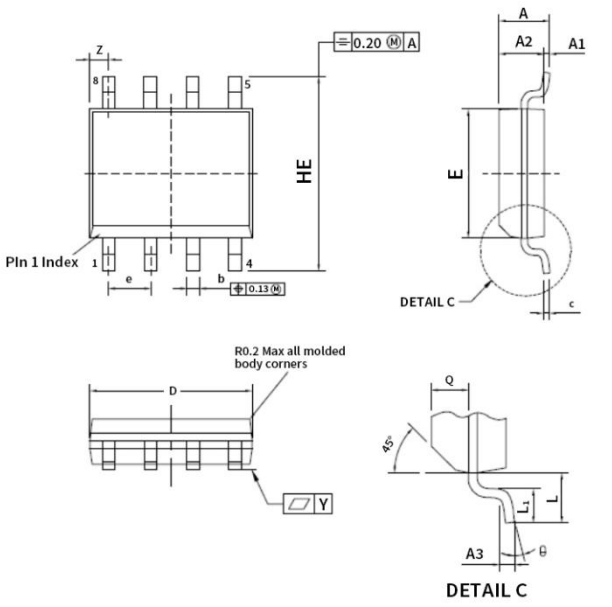
Figure 9.2 Interlock Protection using NSI6601M

9.3. PCB Layout

Careful PCB layout is essential for optimal performance. Some key guidelines are:

- The bypass capacitors should be placed close to NSI6601, between V_{CC1} to GND1, or V_{CC2} to V_{EE2}.
- There is high switching current that charges and discharges the gate of external power transistor, leading to EMI and ring issues. The parasitic inductance of this loop should be minimized, by decreasing loop area and place NSI6601 close to power transistor.
- Place large amount of copper connecting to V_{EE2} pin and V_{CC2} pin for thermal dissipation, with priority on V_{EE2} pin. If the system has multi V_{EE2} or V_{CC2} layers, use multiple vias of adequate size for connection.
- To ensure isolation performance between primary and secondary side, the space under the chip should keep free from planes, traces, pads or via.

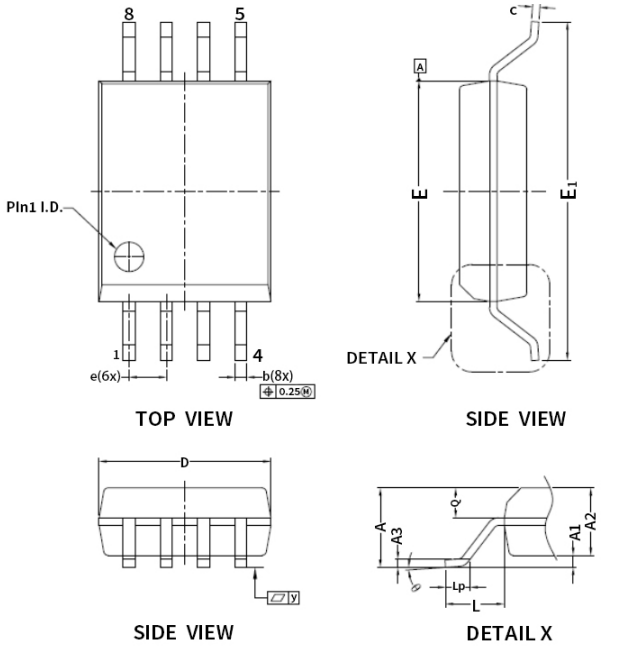
10. Package Information



* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	1.75
A1	0.10	---	0.25
A2	1.25	1.35	1.45
b	0.33	0.38	0.49
c	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
Q	0.60	0.65	0.70
HE	5.80	6.00	6.20
e	1.27 BSC		
L	1.05 BSC		
L1	0.40	0.64	1.00
Y	---	0.10	---
Z	0.3	0.5	0.7
A3	0.25 BSC		
θ	0°	5°	8°

Figure 10.1 SOP8 Package Shape and Dimension in millimeters



* CONTROLLING DIMENSION:MM

SYMBOL	MILLIMETER		
	MIN.	NOM.	MAX.
A	---	---	2.80
A1	0.36	---	0.46
A2	2.20	2.30	2.40
A3	---	0.25	---
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	---	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	---	1.00
y	---	0.10	---
θ	0°	---	8°

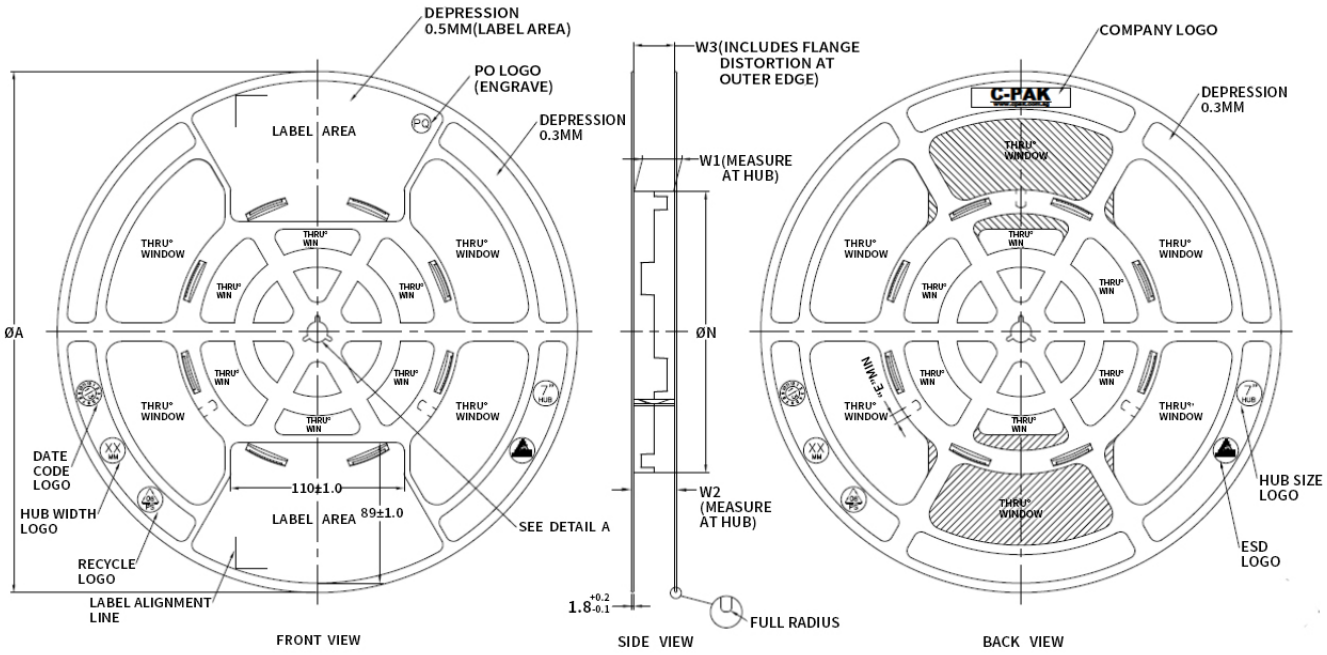
NOTES
1.0 COPWNARITY APPUES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

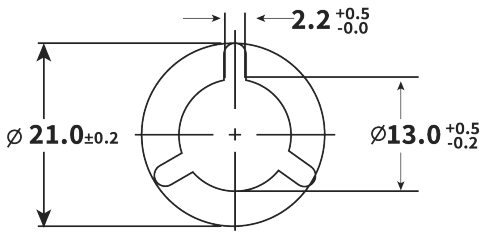
Figure 10.2 SOW8 Package Shape and Dimension in millimeters

11. Ordering Information

Part Number	*Isolation Rating (V)*	*UVLO Level*	*Temperature*	*MSL*	*Package Type*	*Category*	*SPQ*
NSI6601MB-Q1SWVR	5700	9V	-40 to 125°C	3	SOW8	Automotive	1000
NSI6601MC-Q1SWVR	5700	12V	-40 to 125°C	3	SOW8	Automotive	1000
NSI6601MB-Q1SPR	3000	9V	-40 to 125°C	1	SOP8	Automotive	2500
NSI6601MC-Q1SPR	3000	12V	-40 to 125°C	1	SOP8	Automotive	2500
NSI6601WC-Q1SWVR	5700	12V	-40 to 125°C	3	SOW8	Automotive	1000

12. Tape and Reel Information



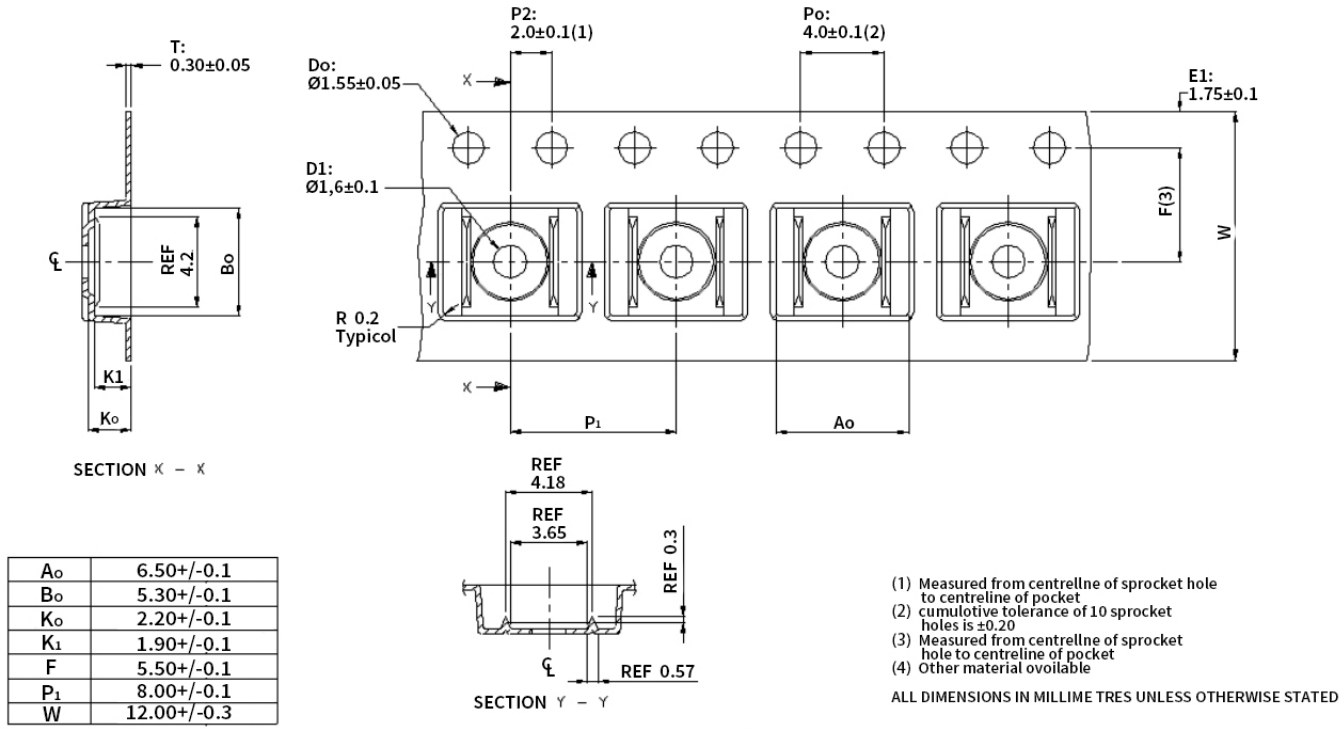


ARBOR HOLE
DETAIL A
SCALE: 3:1

PRODUCT SPECIFICATION						
TAPE WIDTH	ØA ±2.0	ØN ±2.0	W1	W2 (Max)	W3	E (MIN)
08MM	330	178	8.4 +1.5 -0.0	14.4	SHALL ACCOMMODATE TAPE WIDTH WITHOUT NTERFERENCE	5.5
12MM	330	178	12.4 +2.0 -0.0	18.4		5.5
16MM	330	178	16.4 +2.0 -0.0	22.4		5.5
24MM	330	178	24.4 +2.0 -0.0	30.4		5.5
32MM	330	178	32.4 +2.0 -0.0	38.4		5.5

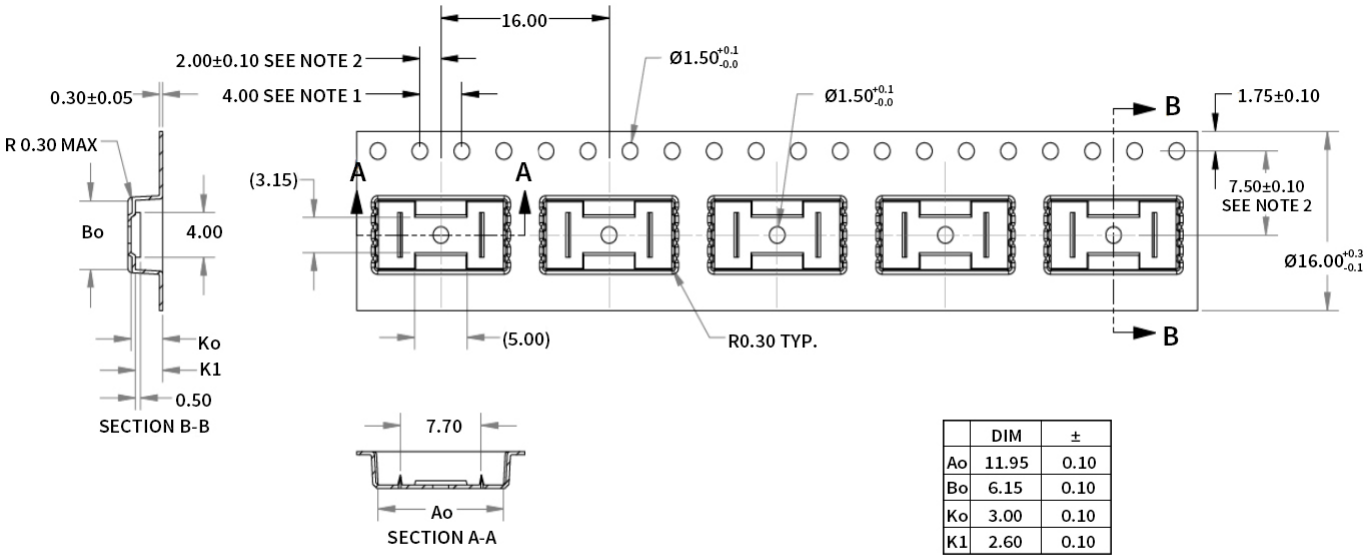
SURFACE RESISTIVITY			
LEGEND	SR RANGE	TYPE	COLOUR
A	BELOW 10^{12}	ANTISTATIC	ALL TYPES
B	10^{6} TO 10^{11}	STATIC DISSIPATIVE	BLACK ONLY
C	10^{5} & BELOW 10^{5}	CONDUCTIVE(GENERIC)	BLACK ONLY
E	10^{9} TO 10^{11}	ANTISTATIC(COATED)	ALL TYPES

Figure 12.1 Tape Information



Ao	6.50+/-0.1
Bo	5.30+/-0.1
Ko	2.20+/-0.1
K1	1.90+/-0.1
F	5.50+/-0.1
P1	8.00+/-0.1
W	12.00+/-0.3

Figure 12.2 Reel Information of SOP8



	DIM	±
Ao	11.95	0.10
Bo	6.15	0.10
Ko	3.00	0.10
K1	2.60	0.10

NOTES:
1.10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2.POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE.
3Ao AND Bo ARE MEASURED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

Figure 12.3 Reel Information of SOW8

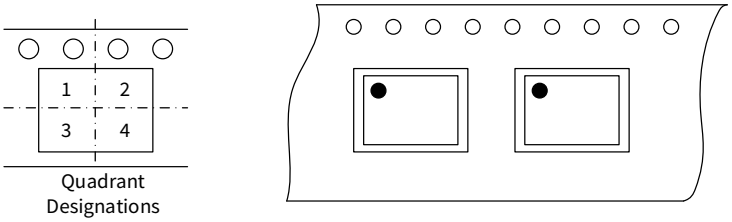


Figure 12.4 Quadrant Designation for Pin1 Orientation in Tape

13. Revision History

Revision	Description	Date
1.0	Initial release	2022/12/22
1.1	1.Modified device information 2.Modified High Voltage Feature Description 3. Modify device name from NSi6601M to NSI6601M 4. Modify SOP8(150mil) to SOP8, SOP8(300mil) to SOW8 5. Change the description of ESD Ratings 6.Update regulation information 7. Modified Figure 9.1 NSI6601M Typical Application Circuit	2023/9/28

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