NOVOSENSE

NSOPA801x-Q1
5.5-V Rail-to-Rail Input/Output 1.5MHz General-Purpose Operational Amplifier

Datasheet (EN) 1.0

Product Overview

The NSOPA801x-Q1 family includes single (NSOPA8011-Q1), dual (NSOPA8012-Q1), and quad-channel (NSOPA8014-Q1), and is a low-voltage (1.8 V to 5.5 V), general purpose, low-power operational amplifiers (op amps) with rail-to-rail input and output swing capabilities. These op amps provide a cost-effective solution for low-voltage operation and high capacitive-load drive are required. The capacitive-load drive of the NSOPA801x-Q1 family is 1 nF, and the resistive open-loop output impedance makes stabilization easier with much higher capacitive loads.

The robust design of the NSOPA801x-Q1 family simplifies circuit design. The op amps feature unity-gain stability, an integrated RFI and EMI rejection filter, and no-phase reversal in overdrive conditions.

Micro-size packages, such as SC70-5, along with industry-standard packages such as SOT23-5L, SOP, MSOP, and TSSOP packages.

Device Information

Part Number	*Package*	*Body Size*
NSOPA8011-Q1STAR	SOT23-5L	2.90 mm × 1.60 mm
NSOPA8011-Q1SCAR	SC70-5	2.07 mm × 1.26 mm
NSOPA8012-Q1SPR	SOP8	4.90 mm × 3.90 mm
NSOPA8012-Q1MSR	MSOP8	3.00 mm × 3.00 mm
NSOPA8014-Q1SPKR	SOP14	8.65 mm × 3.90 mm
NSOPA8014-Q1TSKR	TSSOP14	5.00 mm × 4.40 mm

Typical Application

- Motor control and HEV/EV inverter
- On-board (OBC) and wireless charger
- Body electronics and lighting
- Low-side current sensing
- Advanced driver assistance system (ADAS)

Key Features

- Optimized for AEC-Q100 grade1 application
- Supply voltage range: 1.8V to 5.5V
- Rail-to-rail input and output
- Low input offset voltage: ±0.55 mV (typical)
- Low offset voltage drift: 0.7 μV/°C (typical)
- Gain-bandwidth product: 1.5 MHz (typical)
- Unity-gain stable
- High power supply rejection: 104 dB (typical)
- Low broadband noise: 22 nV/√Hz (typical)
- Low quiescent current: 77 μA/Ch (typical)
- Internal RFI and EMI filter
- Extended temperature range: –40°C to 125°C
- RoHS and REACH Compliance

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1. Pin Configuration and Function

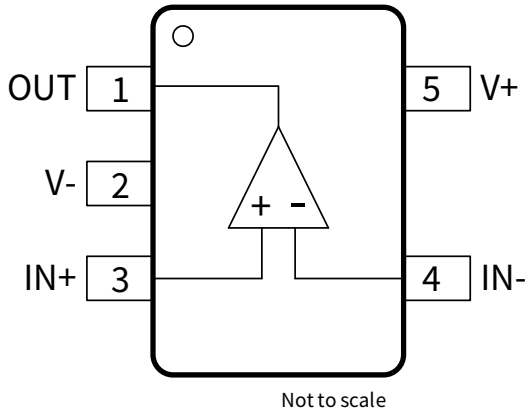


Figure 1-1 NSOPA8011-Q1 5-Pin SOT23 Package Top View

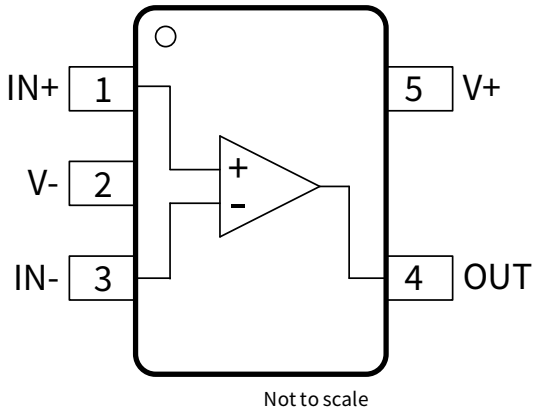


Figure 1-2 NSOPA8011-Q1 5-Pin SC70 Package Top View

Table 1-1 NSOPA8011-Q1 Pin Configuration and Description

Symbol	*NO.*		*Function*
	5-Pin SOT23	**5-Pin SC70**	
IN+	3	1	Noninverting Input
IN-	4	3	Inverting Input
OUT	1	4	Output
V+	5	5	Positive Power Supply
V-	2	2	Negative Power Supply

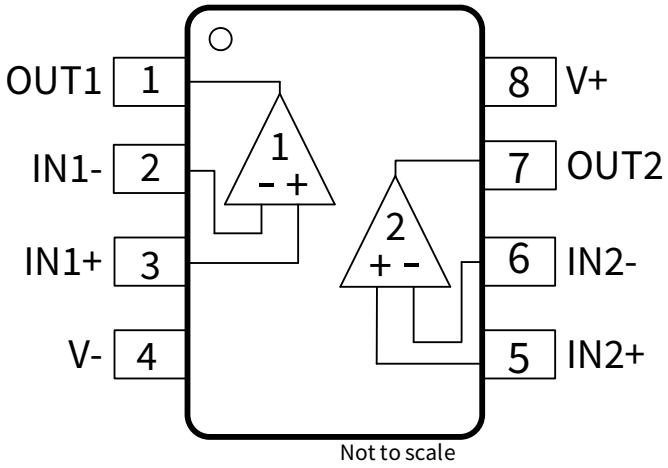


Figure 1-3 NSOPA8012-Q1 8-Pin SOP and MSOP Package Top View

Table 1-2 NSOPA8012-Q1 Pin Configuration and Description

Symbol	*No.*	*Function*
IN1–	2	Channel 1 Inverting Input
IN1+	3	Channel 1 Noninverting Input
OUT1	1	Channel 1 Output
IN2–	6	Channel 2 Inverting Input
IN2+	5	Channel 2 Noninverting Input
OUT2	7	Channel 2 Output
V+	8	Positive Power Supply
V-	4	Negative Power Supply

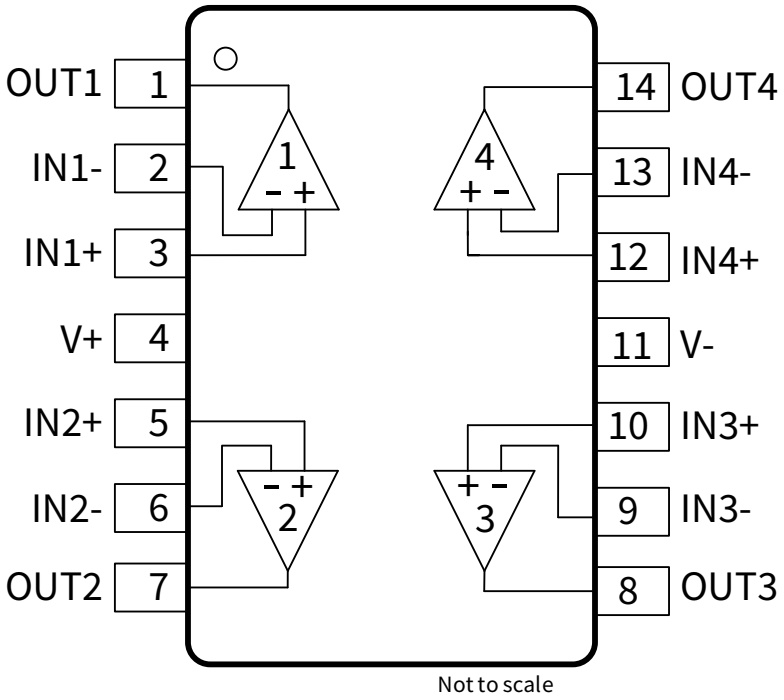


Figure 1-4 NSOPA8014-Q1 14-Pin SOP and TSSOP Package Top View

Table 1-3 NSOPA8014-Q1 Pin Configuration and Description

Symbol	*NO.*	*Function*
IN1–	2	Channel 1 Inverting Input
IN1+	3	Channel 1 Noninverting Input
OUT1	1	Channel 1 Output
IN2–	6	Channel 2 Inverting Input
IN2+	5	Channel 2 Noninverting Input
OUT2	7	Channel 2 Output
IN3–	9	Channel 3 Inverting Input
IN3+	10	Channel 3 Noninverting Input
OUT3	8	Channel 3 Output
IN4–	13	Channel 4 Inverting Input
IN4+	12	Channel 4 Noninverting Input
OUT4	14	Channel 4 Output
V+	4	Positive Power Supply
V-	11	Negative Power Supply

2. Absolute Maximum Ratings[1]

Parameters	Symbol	Min	Max	Unit
Supply voltage $V_S = (V_+) - (V_-)$	V_S	-0.3	7	V
Differential, IN+ to IN− inputs			V_S + 0.2	V
Common-Mode input voltage		(V_-) - 0.5	(V_+) + 0.5	V
Pins Input current		−10	10	mA
Junction temperature	T_J		150	°C
Storage temperature	T_{stg}	−55	150	°C

3. ESD Ratings

Ratings		Value	Unit
Electrostatic discharge	● Human body model (HBM), per AEC Q100-002	±5000	V
	● Charged device model (CDM), per AEC Q100-011	±2000	V

4. Recommended Operating Conditions

Parameters	Symbol	Min	Max	Unit
Supply voltage	V_S	1.8	5.5	V
Operating free-air temperature	T_A	-40	125	°C

5. Thermal Information

Parameters	Symbol	SOT23-5L	SC70-5	SOP8	MSOP8	SOP14	TSSOP14	Unit
IC Junction-to-Air thermal resistance	θ_{JA}	232.9	239.6	207.9	201.2	102.1	148.3	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(TOP)}$	153.8	148.5	92.8	85.7	56.8	68.1	°C/W
Junction-to-board thermal resistance	θ_{JB}	100.9	82.3	129.7	122.9	58.5	92.7	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	77.2	54.5	26	21.2	20.5	16.9	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	100.4	81.8	127.9	121.4	58.1	91.8	°C/W

[1] Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability

6. Electrical Characteristics

For V_S = (V_+) – (V_-) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V) at T_A = 25 °C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

Parameters	*Symbol*	*Condition*		*Min*	*Typ*	*Max*	*Unit*
INPUT							
Offset voltage	V_{OS}	V_S = 5.5 V	T_A = 25°C		±0.55	±3.2	mV
			T_A = –40°C to 125°C			±3.5	
Offset voltage Drift	dV_{OS}/dT	T_A = –40 °C to 125 °C			±0.7		µV/°C
Common-mode input range	V_{CM}			(V_-)-0.2		(V_+)+0.2	V
Common mode rejection ratio	CMRR	V_S = 1.8 V, (V_-) – 0.2 V < V_{CM} < (V_+) – 1.4 V (PMOS pair)	T_A = 25°C		89		dB
			T_A = –40°C to 125°C		88		
		V_S = 5.5 V, (V_-) – 0.2 V < V_{CM} < (V_+) - 1.4 V (PMOS pair)	T_A = 25°C	83	99		
			TA = –40°C to 125°C	81			
		V_S = 1.8 V, (V_-) – 0.2 V < V_{CM} < (V_+) + 0.2 V	T_A = 25°C		70		
			TA = –40°C to 125°C		69		
		V_S = 5.5 V, (V_-) – 0.2 V < V_{CM} < (V_+) + 0.2 V	T_A = 25°C	61	79		
			TA = –40°C to 125°C	60			
Channel Separation		f = 0Hz			120		dB
Input bias current	I_B	V_S = 1.8 V to 5.5 V, V_{CM} = V_S/2			±5		pA
Input offset current	I_{OS}	V_S = 1.8 V to 5.5 V, V_{CM} = V_S/2			±5		
Input Impedance	Z_{ID}	Differential			0.13||4		TΩ||pF
	Z_{ICM}	Common-mode			1||5		
OPEN-LOOP GAIN							
Open-loop voltage gain	A_{OL}	V_S = 1.8V, R_L=10kΩ, (V_-)+0.05V<V_O<(V_+)–0.05V			110		dB
		V_S = 5.5V, R_L=10kΩ, (V_-)+0.05V<V_O<(V_+)–0.05V		105	118		
		V_S = 1.8V, R_L=2kΩ, (V_-) +0.15V<V_O<(V_+)–0.15V			112		
		V_S = 5.5V, R_L=2kΩ, (V_-) +0.15V<V_O<(V_+)–0.15V			129		

Electrical Characteristics (continued)

For V_S = (V_+) – (V_-) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S/2, V_{CM} = V_S/2, and V_{OUT} = V_S/2, unless otherwise noted.

Parameters	Symbol	Condition		Min	Typ	Max	Unit
OUTPUT							
Output swing from rail headroom	V_O	V_S=1.8 V, R_L=10 kΩ			3.5		mV
		V_S=5.5 V, R_L=10 kΩ			6	10	
		V_S=1.8 V, R_L=2 kΩ			16		
		V_S=5.5 V, R_L=2 kΩ			28	32	
Short-Circuit Current	I_{SC}	V_S=5.5 V, Sinking			63		mA
		V_S=5.5 V, Sourcing			55		
Output Impedance	Z_O	f = 1 MHz, I_O = 0 A			705		Ω
FREQUENCY RESPONSE							
Gain-bandwidth product	GBP	V_S = 5.5 V, C_L = 10 pF			1.5		MHz
Phase margin	PM	V_S = 5.5 V, C_L = 10 pF			70		Degree
Settling time	T_S	To 0.1%, V_S = 5 V, 2 V Step, C_L = 100 pF			3		µs
		To 0.01%, V_S = 5 V, 2 V Step, C_L = 100 pF			3.7		
		To 0.1%, V_S = 1.8 V, 1.5 V Step, C_L = 100 pF			4.7		
		To 0.01%, V_S = 1.8 V, 1.5 V Step, C_L = 100 pF			5.4		
Slew rate	SR	V_S = 5.5 V, 3V step, G= +1			2		V/µs
Total harmonic distortion + noise	THD+N	V_{rms} = 1 V, G = 1, f = 1 kHz, R_L= 10kΩ			95		dB
Overload recovery time		V_{IN} × Gain > V_S			1		µs
EMI rejection ratio	EMIRR	f = 1GHz			60		dB
NOISE (INPUT REFERRED)							
Input voltage noise density	e_n	f = 1 kHz			28		nV/$\sqrt{Hz}$
		f = 10 kHz			22		
Input Voltage noise	$e_{n\ p\text{-}p}$	f = 0.1 Hz to 10 Hz			4		µVpp
POWER SUPPLY							
Operating voltage range	V_S			1.8		5.5	V
Power supply rejection ratio	PSRR	V_S = 1.8 V to 5.5 V, V_{CM} = (V-)	T_A = 25°C	89	104		dB
			T_A = –40 °C to 125 °C	84			
Quiescent current per amplifier	I_Q	V_S=1.8 V	T_A = 25°C		59	94	µA
			T_A = –40 °C to 125 °C			135	
		V_S=5.5 V	T_A = 25°C		77	120	
			T_A = –40 °C to 125 °C			150	

7. Typical Performance Characteristics

For $V_S = (V_+) - (V_-) = 5.5$ V (±2.75 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

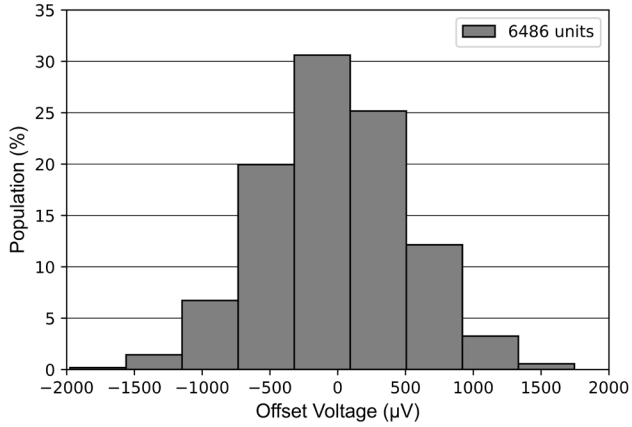


Figure 7-1 Offset Voltage Production Distribution

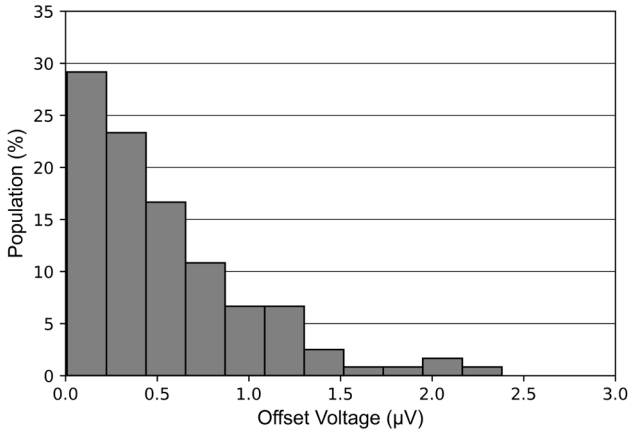


Figure 7-2 Offset Voltage Drift Distribution

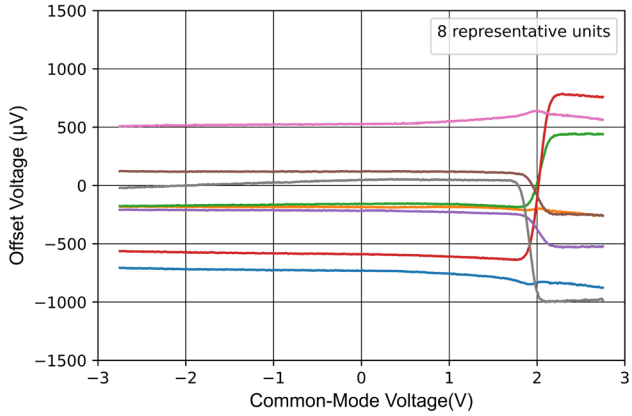


Figure 7-3 Offset Voltage vs Common-Mode Voltage

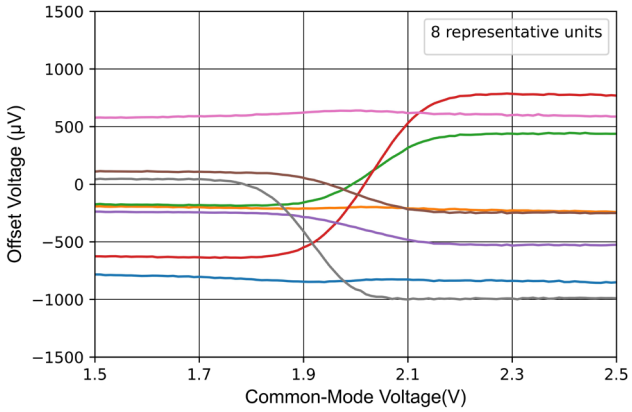


Figure 7-4 Offset Voltage vs Common-Mode Voltage (Transition Region)

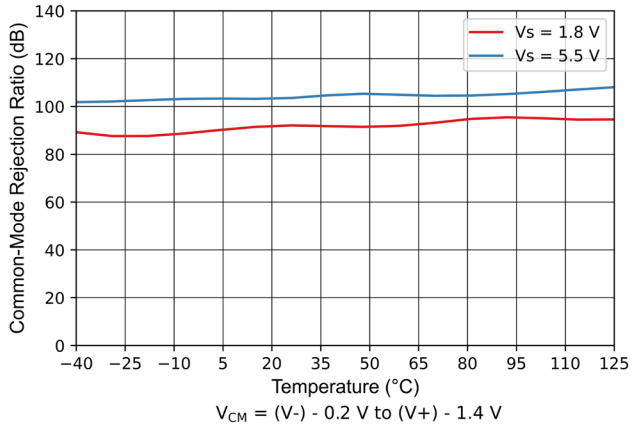


Figure 7-5 CMRR vs Temperature

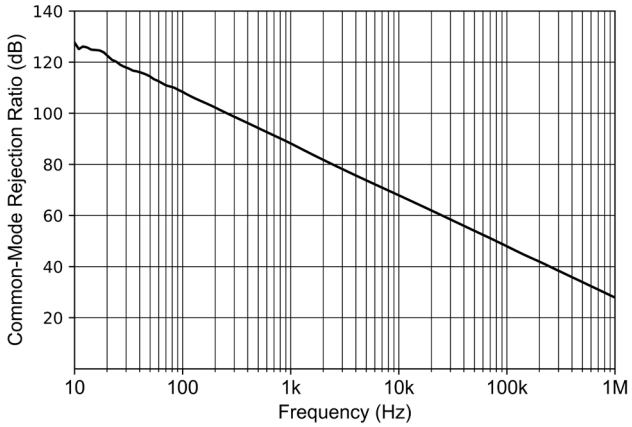


Figure 7-6 Common-Mode Rejection Ratio vs Frequency

Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 5.5$ V (±2.75 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

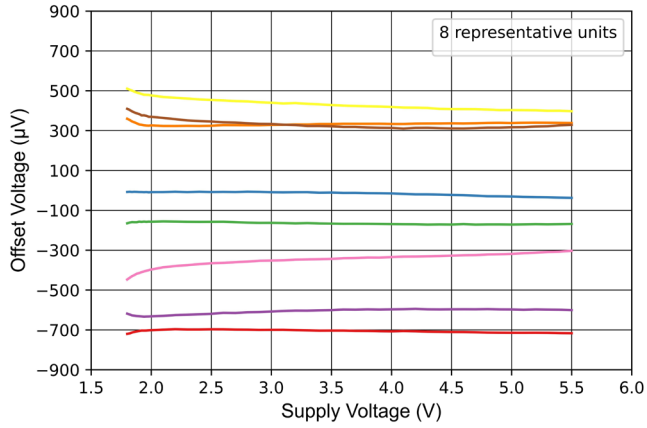


Figure 7-7 Offset Voltage vs Power Supply

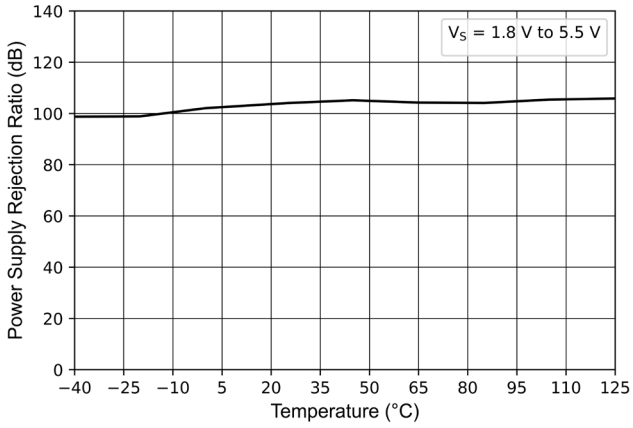


Figure 7-8 PSRR vs Temperature

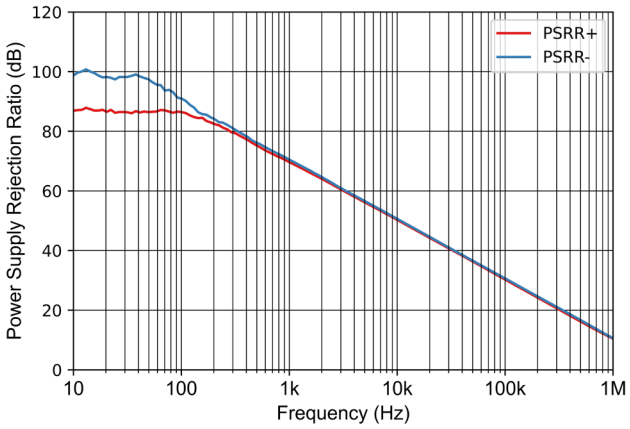


Figure 7-9 Power-Supply Rejection Ratio vs Frequency

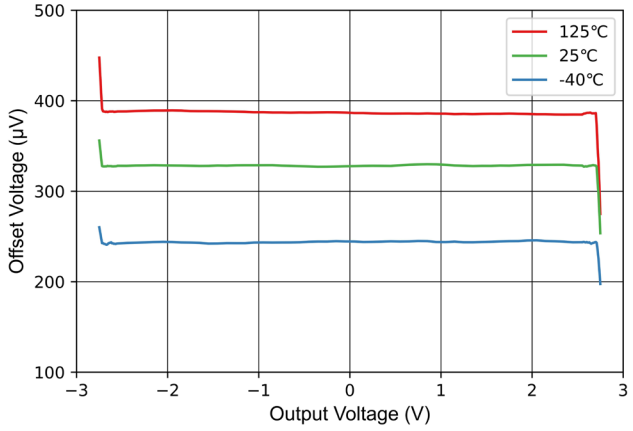


Figure 7-10 Offset Voltage vs Output Voltage

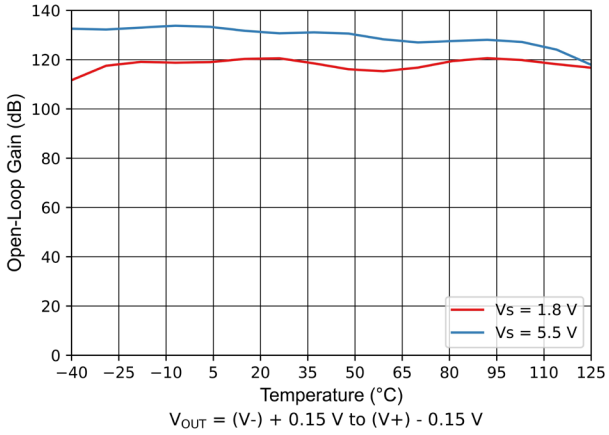


Figure 7-11 Open-Loop Gain vs Temperature

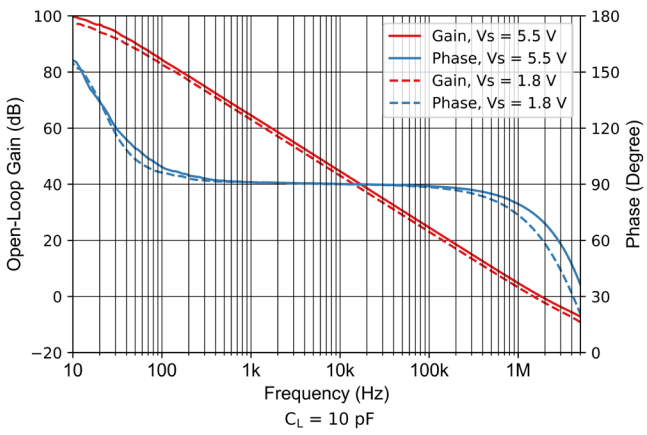


Figure 7-12 Open Loop Gain vs Frequency

Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 5.5$ V (±2.75 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

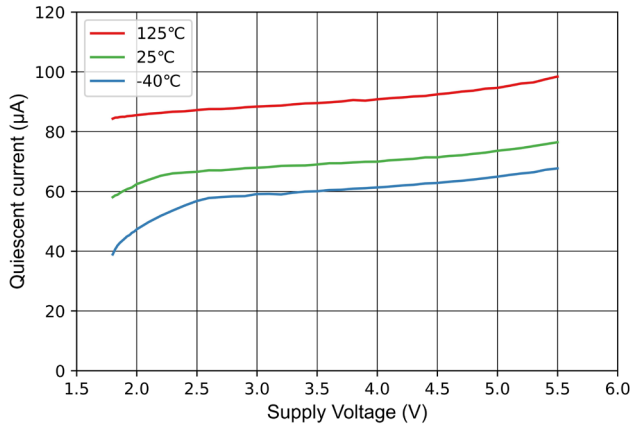


Figure 7-13 Quiescent Current vs Supply Voltage

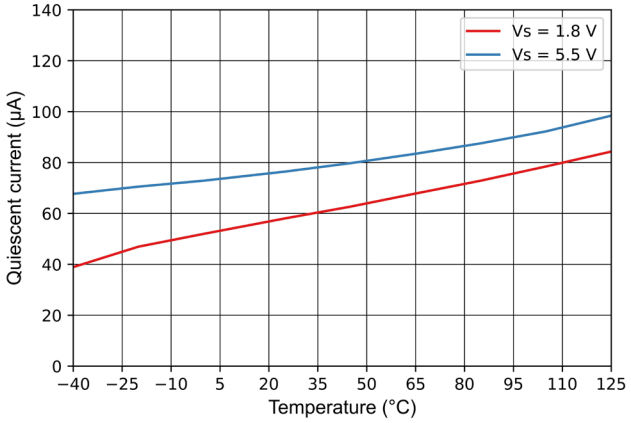


Figure 7-14 Quiescent Current vs Temperature

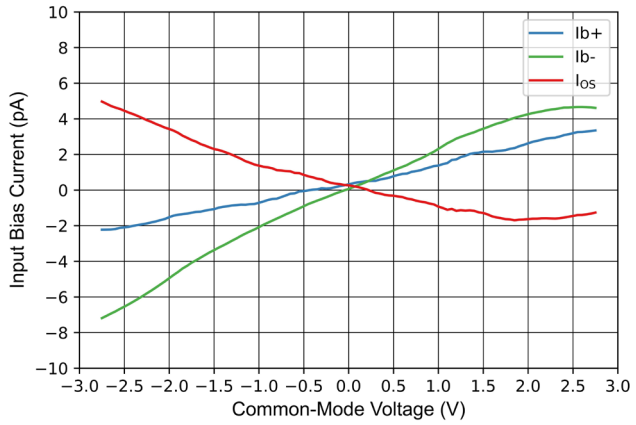


Figure 7-15 Input Bias Current vs Common-Mode Voltage

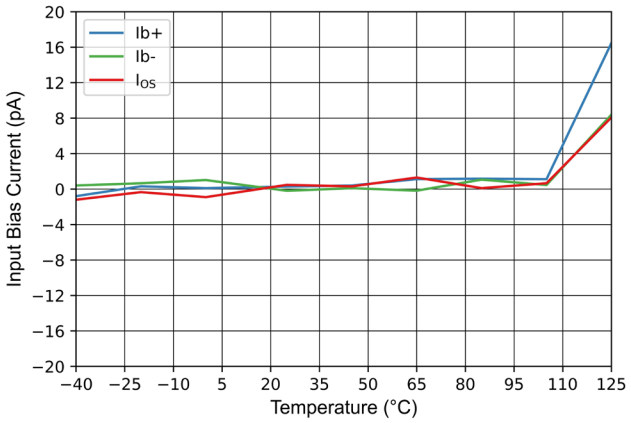


Figure 7-16 Input Bias Current vs Temperature

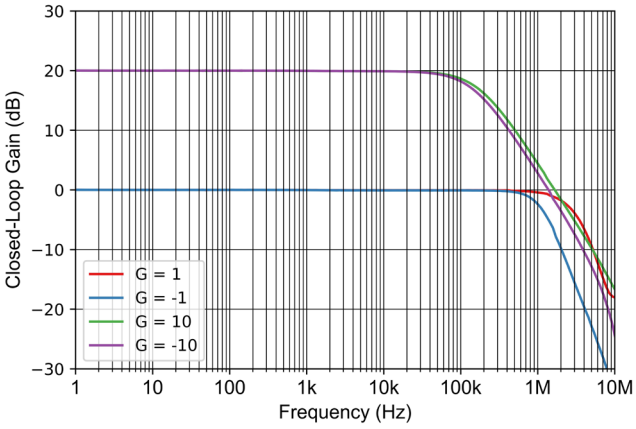


Figure 7-17 Closed Loop Gain vs Frequency

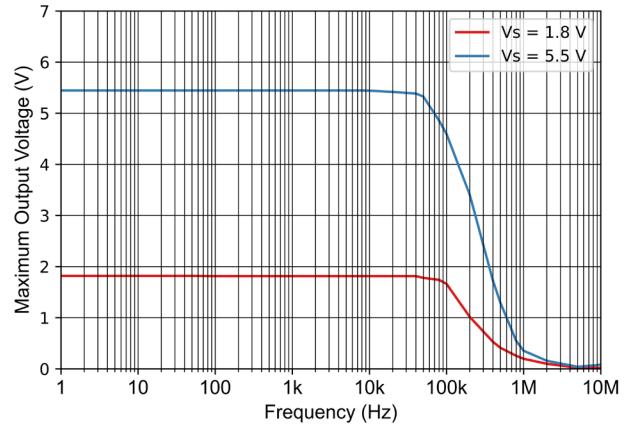


Figure 7-18 Maximum Output Voltage vs Frequency

Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 5.5$ V (±2.75 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

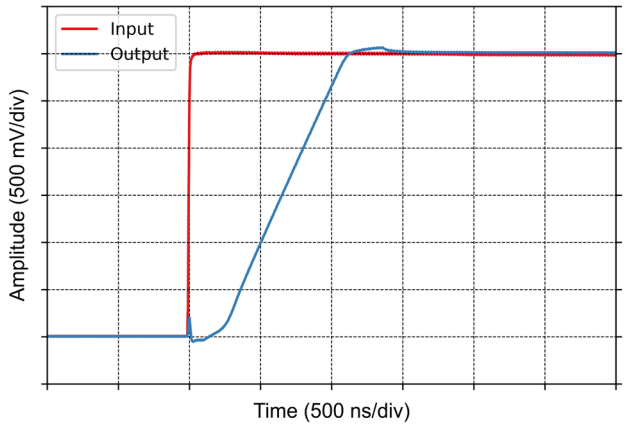


Figure 7-19 Large-Signal Step Response (Rising)

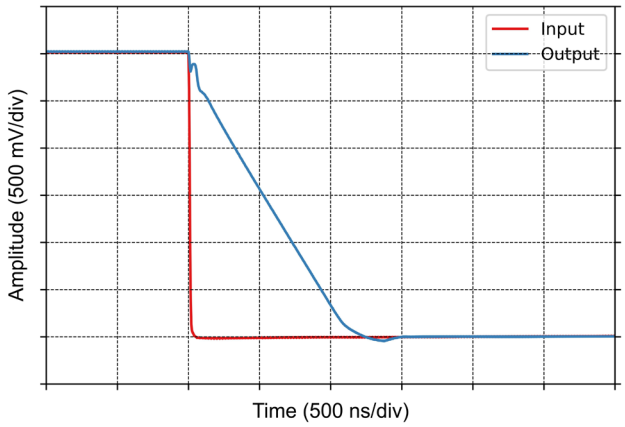


Figure 7-20 Large-Signal Step Response (Falling)

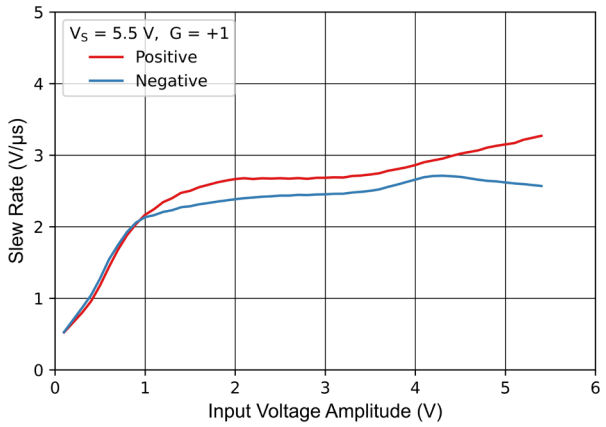


Figure 7-21 Slew Rate vs Input Voltage Amplitude

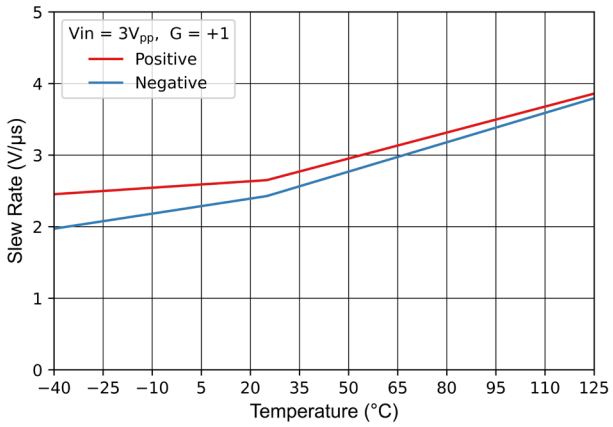


Figure 7-22 Slew Rate vs Temperature

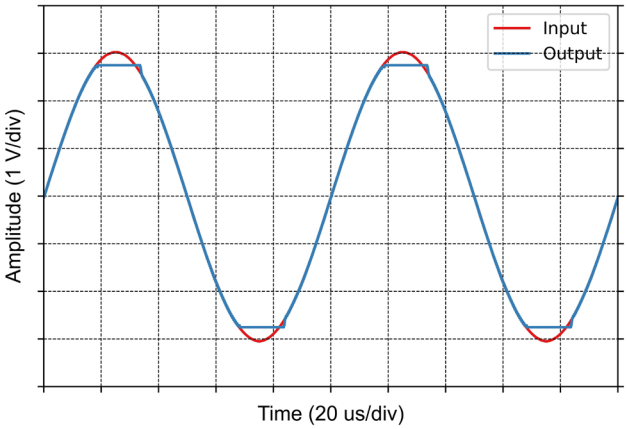


Figure 7-23 No Phase Reversal

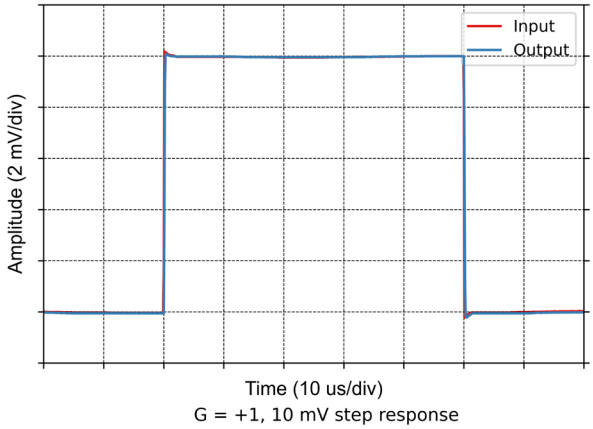


Figure 7-24 Small-Signal Step Response

Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 5.5$ V (±2.75 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

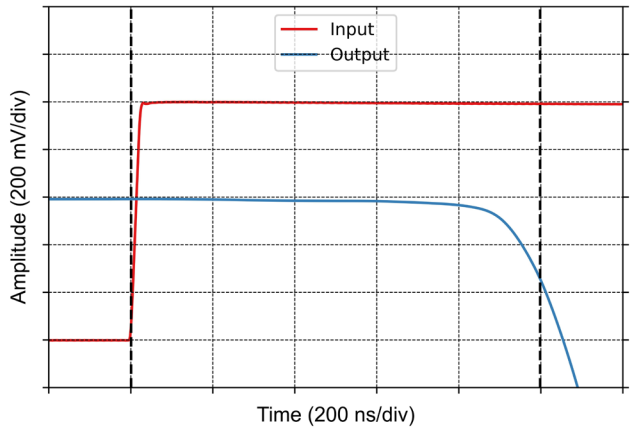


Figure 7-25 Positive Overload Recovery (G = -10)

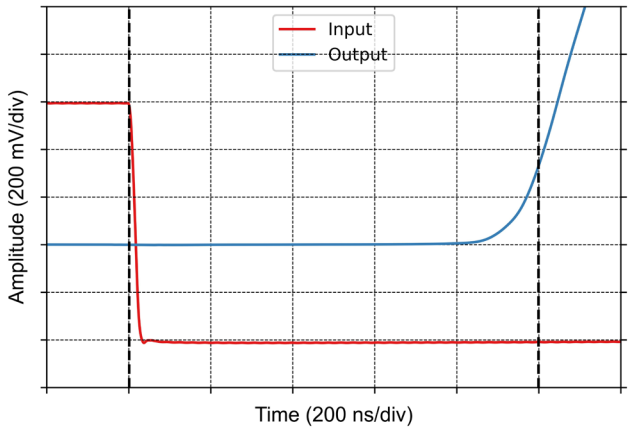


Figure 7-26 Negative Overload Recovery (G = -10)

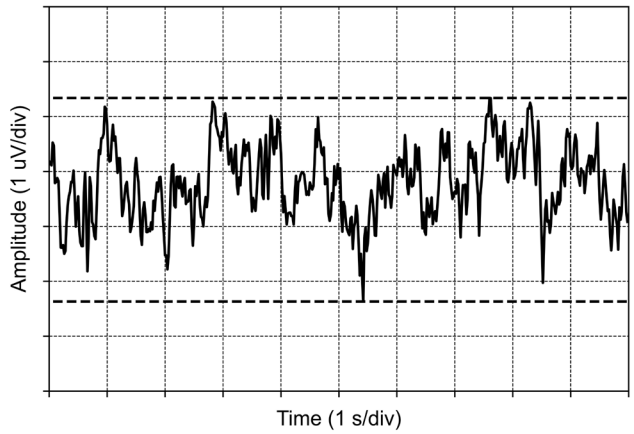


Figure 7-27 0.1-Hz to 10-Hz Noise

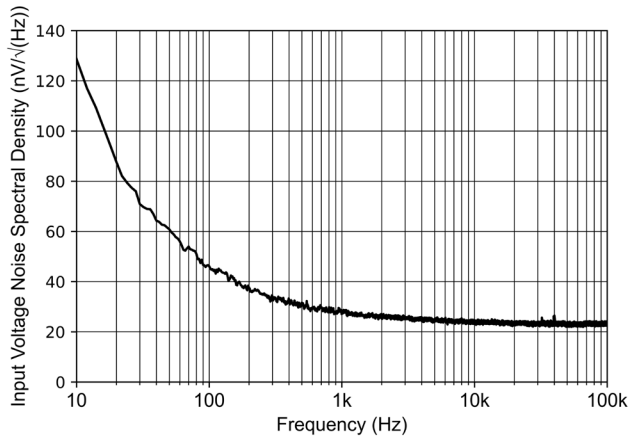


Figure 7-28 Input Voltage Noise Spectral Density

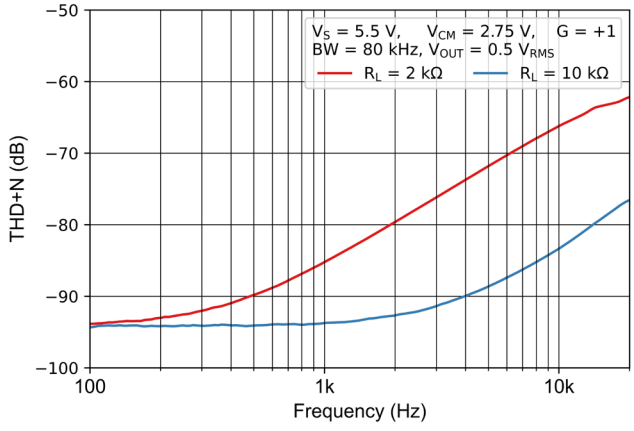


Figure 7-29 THD+N Ratio vs Frequency

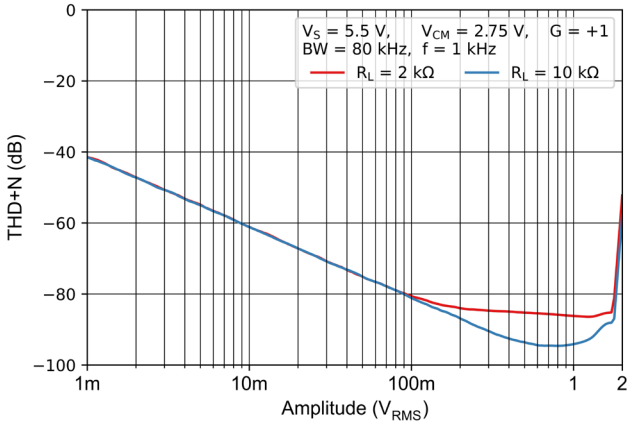


Figure 7-30 THD+N vs Output Amplitude

Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 5.5$ V (±2.75 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

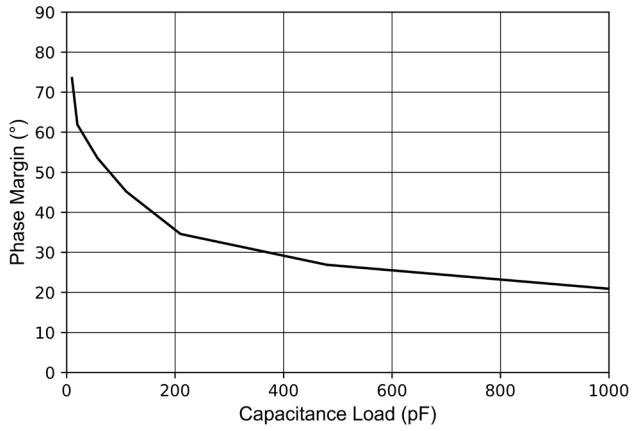


Figure 7-31 Phase Margin vs Capacitive Load

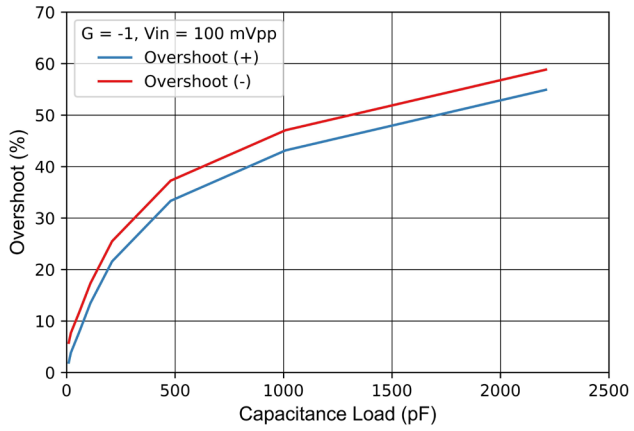


Figure 7-32 Small-Signal Overshoot vs Capacitive Load

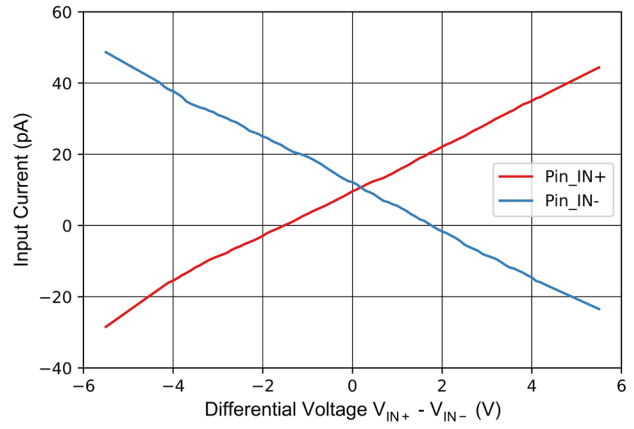


Figure 7-33 Input Current vs Differential Voltage(V_{IN+} - V_{IN-})

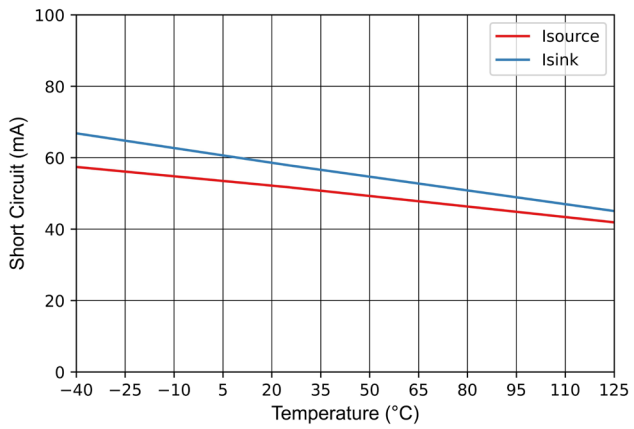


Figure 7-34 Short-Circuit vs Temperature

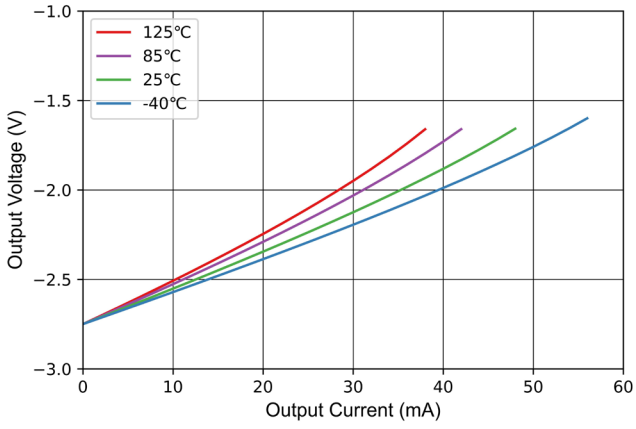


Figure 7-35 Output Voltage Swing vs Output Sinking Current

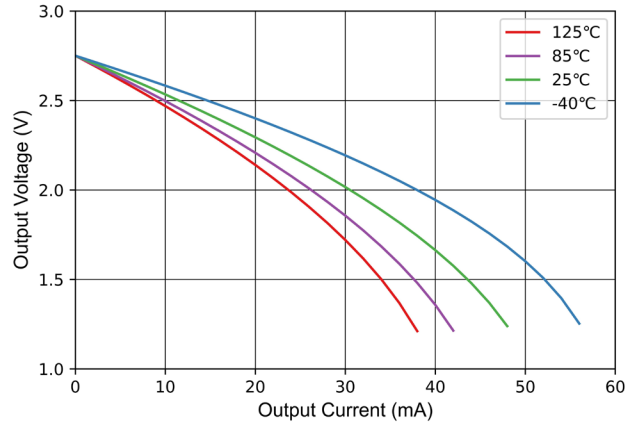


Figure 7-36 Output Voltage Swing vs Output Sourcing Current

Typical Performance Characteristics (continued)

For $V_S = (V_+) - (V_-) = 5.5$ V (±2.75 V) at $T_A = 25°C$, $R_L = 10$ kΩ connected to $V_S/2$, $V_{CM} = V_S/2$, and $V_{OUT} = V_S/2$, unless otherwise noted.

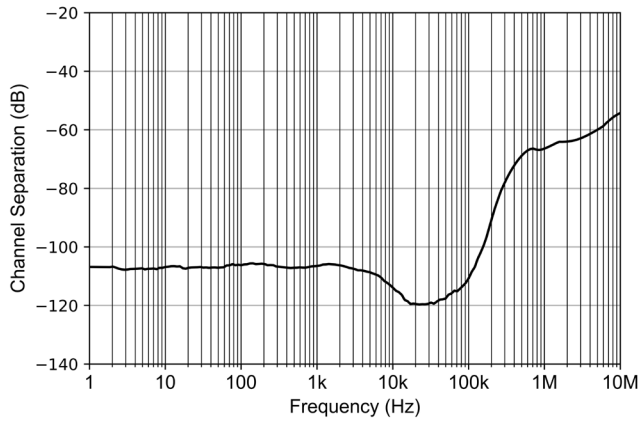


Figure 7-37 Channel Separation vs Frequency

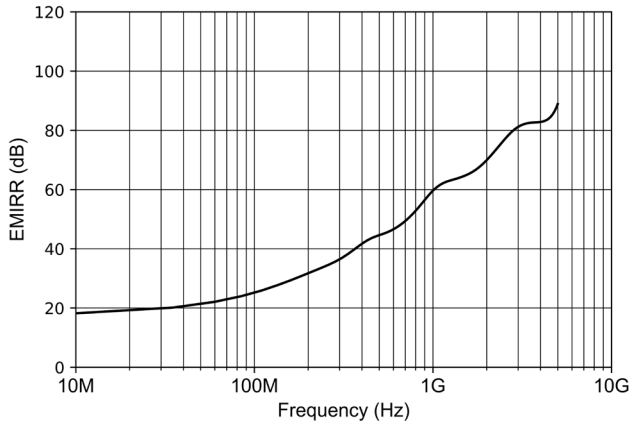


Figure 7-38 EMIRR vs Frequency

8. Detailed Description

8.1 Overview

The NSOPA801x-Q1 is a family of rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the NSOPA801x-Q1 family to be used in virtually any single-supply application.

8.2 Function Block

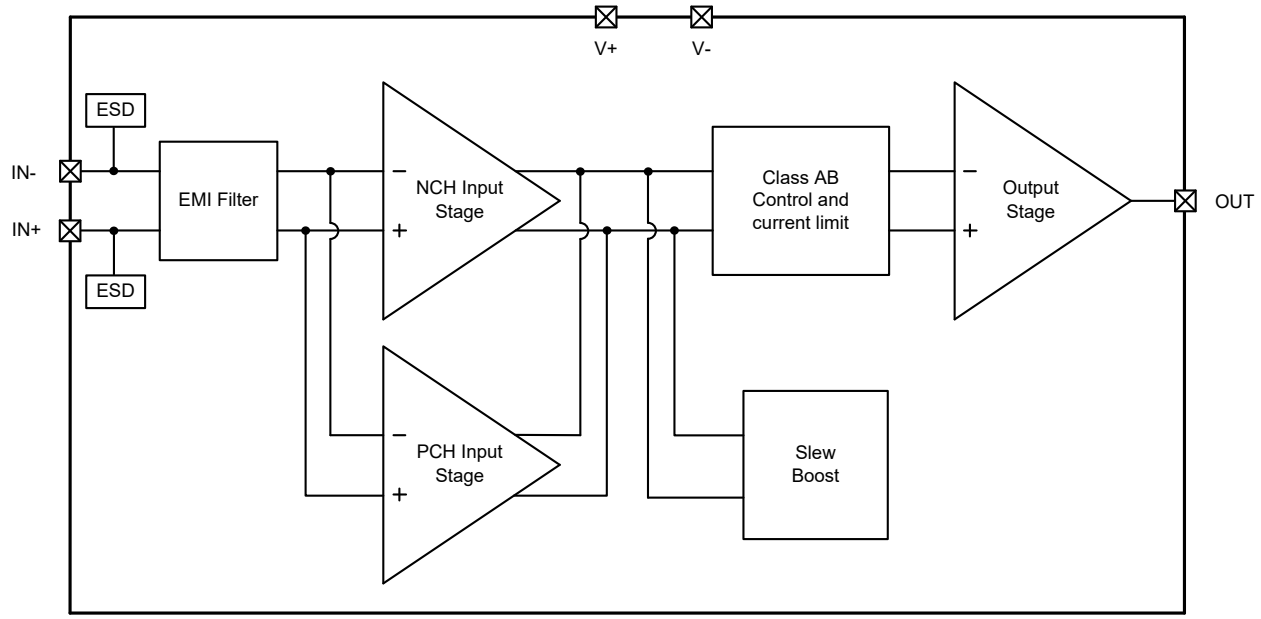


Figure 8-1 NSOPA801x-Q1 Functional Block Diagram (One channel is shown)

8.3 Feature Description

8.3.1 Common-Mode Input Stage

The NSOPA801x-Q1 is a 5.5V true rail-to-rail input op amp with an input common-mode range of 200mV beyond either supply rail. This wide range is achieved by paralleling complementary N-channel and P-channel differential input pairs, as shown in Figure 8-2.

N-channel pairs are active when the input voltage is close to the positive power rail, typically ranging from 200 mV higher than the positive power (V+) to 500 mV lower than (V+). The P-channel pair is active over an input range from 200 mV below the negative supply to approximately (V+) – 1.0 V. There is a small transition region, typically (V+) – 1.0 V to (V+) – 0.5 V, where both input pairs are on. This transition region will vary slightly with process variations, and within this region, PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

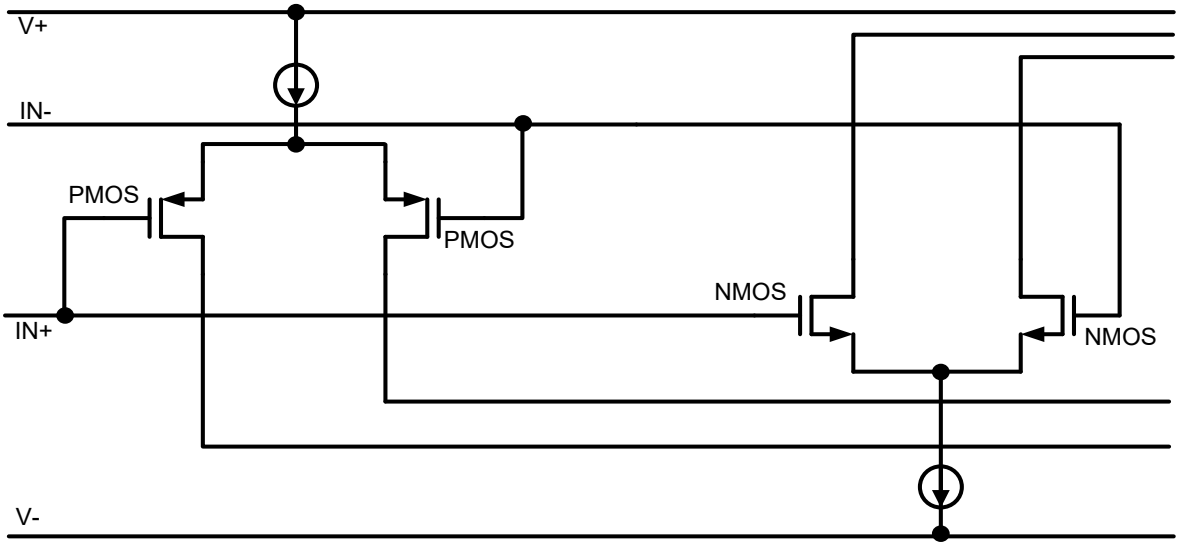


Figure 8-2 Rail-to-rail Input Stage

8.3.2 Slew Rate Boost

NSOPA801x-Q1 has internal SR boost block. The boost circuit can provide positive and negative current flow to boost both positive and negative slew rates. Actually, the slew rate of device depends on the input amplitude voltage. The figure illustrates the behavior of this feature.

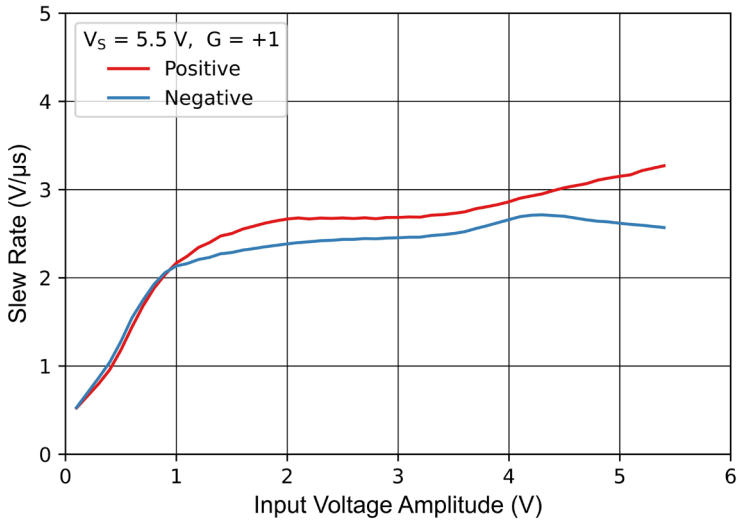


Figure 8-3 Slew-Rate vs Input Voltage Amplitude

8.3.3 EMIRR

The NSOPA801x-Q1 series use integrated electromagnetic interference (EMI) filtering to reduce the impact of EMI on devices such as wireless communications and dense circuit boards that mix analog signal chains and digital components. EMI immunity can be improved through circuit design technology; the advantage of NSOPA801x-Q1 lies in these design improvements, making EMIRR=60dB@1GHz. Figure 8-4 shows the EMIRR IN+ values for the NSOPA801x-Q1 at articular frequencies commonly encountered in real-world applications.

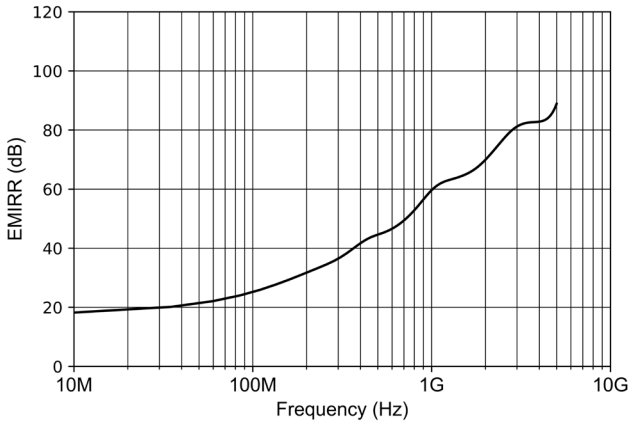


Figure 8-4 EMIRR vs Frequency

8.3.4 Drive Capacitive Load

The NSOPA801x-Q1 has a resistive output stage capable of driving moderate capacitive loads, and by utilizing isolation resistors, the device can be easily configured to drive large capacitive loads. The specific OP amp circuit configuration, layout, gain, and output loading are important factors in determining whether the amplifier will operate stably Some factors to consider.

To obtain additional drive capability in a unity-gain configuration, capacitive load drive can be improved by inserting a small resistor, R_{ISO}, in series with the output, as shown in Figure 8-5. This resistor significantly reduces ringing and maintains DC performance under purely capacitive loads. However, if a resistive load is placed in parallel with a capacitive load, a voltage divider is created, which introduces a gain error at the output and slightly reduces the output swing. The error introduced is proportional to the ratio R_{ISO}/R_L and is usually negligible at low voltage output levels. High capacitive load drive makes the NSOPA801x-Q1 ideally suited for applications such as reference buffers, MOSFET gate drives, and cable shield drives. The circuit shown in Figure 8-5 uses an isolation resistor R_{ISO} to stabilize the op amp output. R_{ISO} modifies the open-loop gain of the system to increase phase margin.

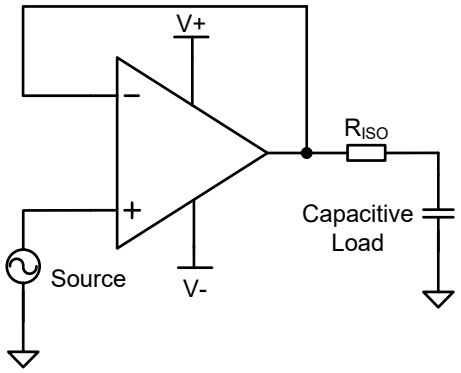


Figure 8-5 Insert Isolation Resistor to Drive Large Capacitive Load

8.3.5 Electrical Overstress

Always, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 8-6 shows an illustration of the ESD circuits contained in the NSOPA801x-Q1 (indicated by the dotted area). The ESD protection circuitry

involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

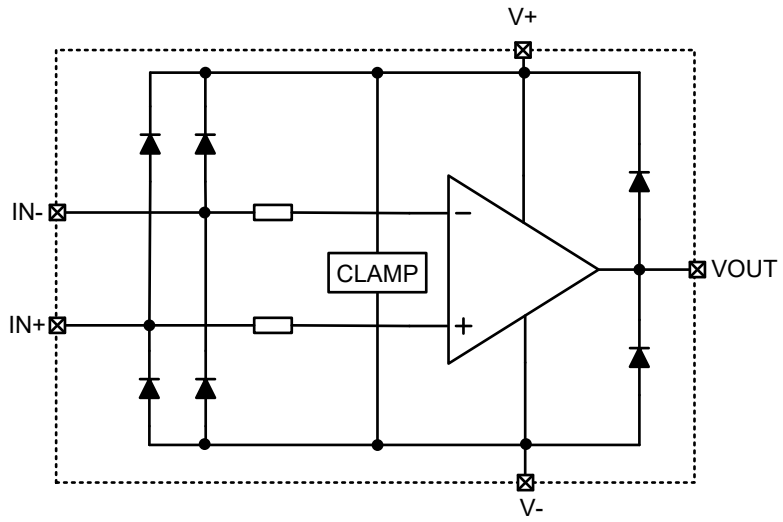


Figure 8-6 Internal ESD Equipment Model

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin.

Electrostatic Discharge (ESD) is defined the transfer of electrostatic charge between bodies or surfaces at different electrostatic potential. ESD is regarded as a high voltage(kV), short duration event(1-100ns). Besides, it is fast edges and lower power event.

But unlike ESD problems, EOS is another common device problem. Electrical Over Stress (EOS) is defined the exposure of an item to current or voltage beyond its maximum ratings.

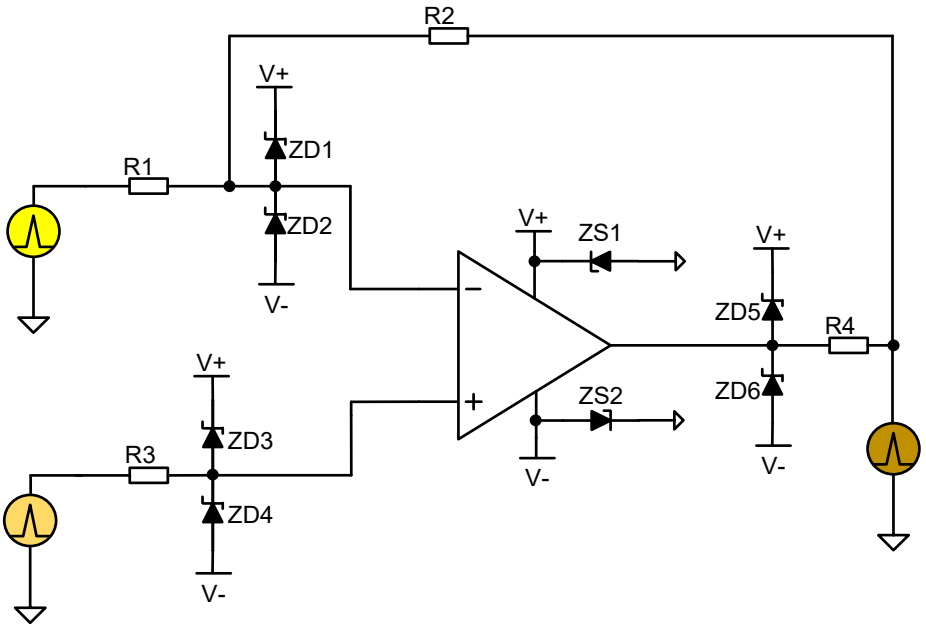


Figure 8-7 External Component to Enhance EOS Performance

Figure 8-7 shows how to use external components to enhance the circuitry robustness.

1. ZDx are small signal Schottky diodes. Using power Schottky for power operational amplifier. Diodes limits EOS Voltage to [(V+) +0.5V] or [(V-)-0.5V].
2. ZS1 and ZS2 are Zener diodes or unipolar semiconductor Transient Voltage Suppressors (TVS). They prevent device supply over-voltage, provide reverse polarity protection, and provide a current path for Iq if one supply floats.
3. R1, R2 limit current through ZD1, ZD2.
4. R3 limits current through ZD3, ZD4.
5. R4 limits current through ZD5, ZD6.R4 is inside the feedback loop adding little error at output voltage.
6. **Check Absolute Maximum Ratings before using devices and never violate the Absolute Maximum Ratings.**

9. Application Information

9.1 Active Filter

NSOPA801x-Q1 can be configured into different types of filters for processing complex signals. Here is a brief explanation of Sallen-key filter type.

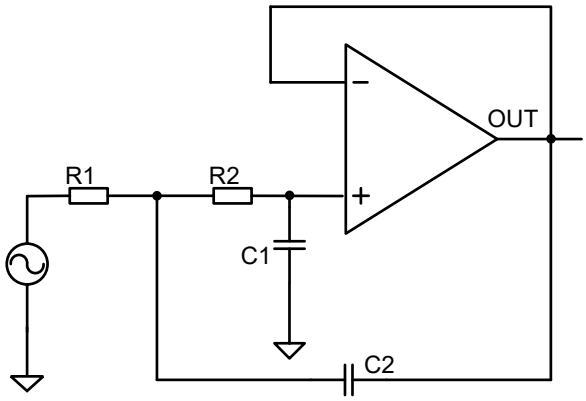


Figure 9-1 Second-Order Sallen-Key Filter

The transfer function of this circuit can be derived as:

$$f_c = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

The 1kHz low pass filter is taken as a design example. By setting R1=9.1kΩ, R2=13 kΩ, C1=10nF and C2=20.5nF, we can get the amplitude-frequency and phase-frequency curves as follows.

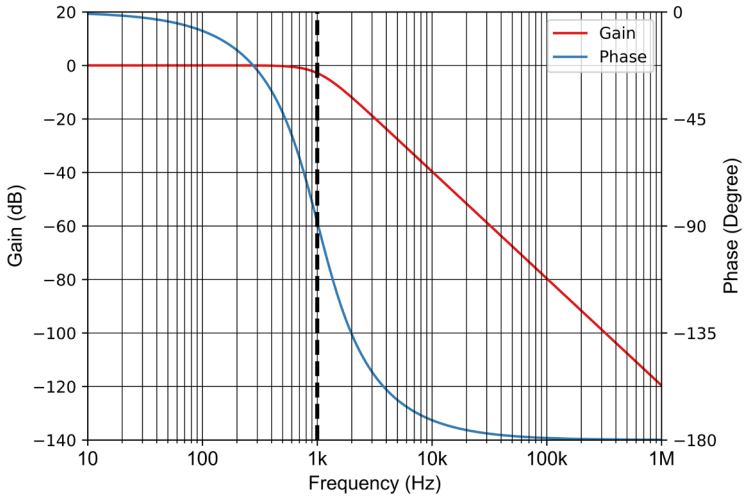


Figure 9-2 Amplitude-Frequency and Phase-Frequency Curves

9.2 Low-Side Current Sensing Application

NSOPA801x-Q1 can be configured in Low-Side Current Sensing. Figure 9-3 shows the applications.

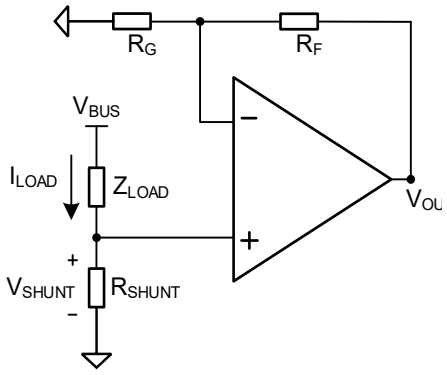


Figure 9-3 NSOPA801x-Q1 in a Low-Side, Current-Sensing Application

The transfer function of this circuit can be derived as:

$$I_{LOAD} = \frac{V_{OUT} \times R_G}{(R_F + R_G) \times R_{SHUNT}}$$

The I_{LOAD} current produces a voltage drop across the R_{SHUNT}. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the NSOPA801x-Q1 to produce an output voltage V_{OUT}, from which the load current can be calculated.

However, it should be noted that select a resistor with the appropriate resistance value. The first is to avoid V_{SHUNT} and V_{OS} orders of magnitude similar, V_{SHUNT} should be much larger than V_{OS}. Because the generated V_{SHUNT} will be relatively small when the I_{LOAD} current is small. At this time, the influence of V_{OS} will dominate, resulting in a large measurement error. Second, the V_{SHUNT} generated when flowing through the maximum I_{LOAD} current does not exceed the common-mode voltage range of NSOPA801x-Q1. It is also necessary to configure the gain reasonably to avoid the phenomenon of the output voltage exceeding the power supply rail.

10.Layout Guidelines

10.1 Guidelines

Poor op amp PCB layout will deteriorate the chip parameters, or even worse, cause it to work abnormally. For better performance, some tips should be considered.

• Noise can propagate into the analog circuitry through the board's power connections and to the power pins of the op amp itself. Bypass capacitors are used to reduce coupled noise by providing a low impedance path to ground.

Connect a low ESR 0.1μF ceramic bypass capacitor between each supply pin and ground as close to the device as possible. A single bypass capacitor from V+ to ground is sufficient for single-supply applications.

• To reduce parasitic coupling, keep input traces as far away from power supply or output traces as possible. If these traces cannot be kept separate, route them at a 90-degree angle

It's much better to run overly sensitive traces than to run traces parallel to noisy traces.

• External components should be located as close to the device as possible, as shown in Figure 10-1. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.

• Keep input traces as short as possible. Remember, the input traces are the most sensitive parts of the circuit.

• For best performance, cleaning is recommended after PCB board assembly.

10.2 Example

A single channel is shown as follow. The rest channels should be handled with identical way but not shown in the figure.

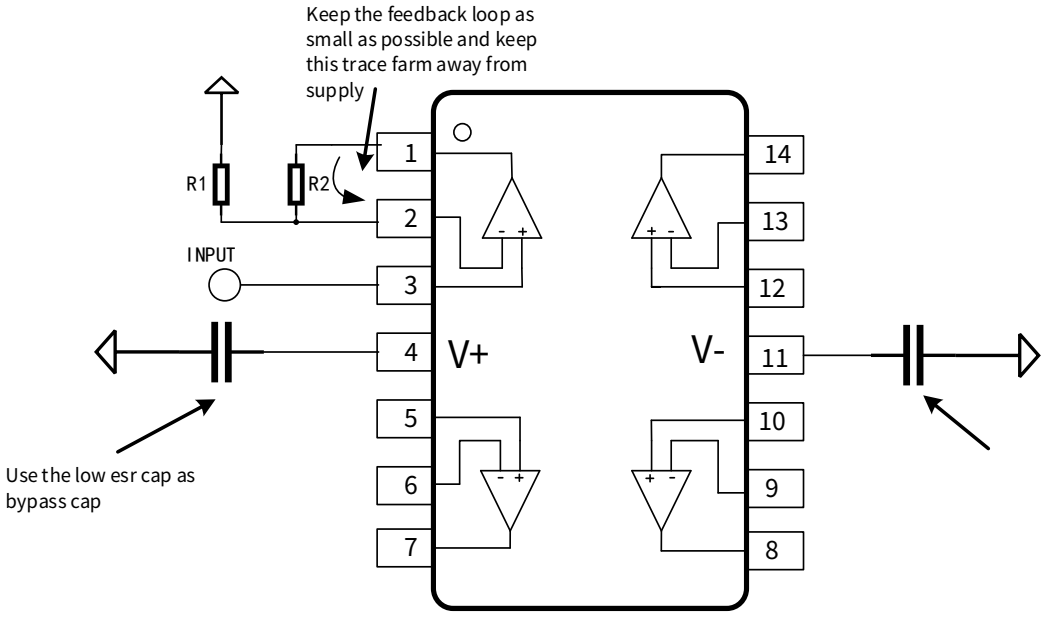
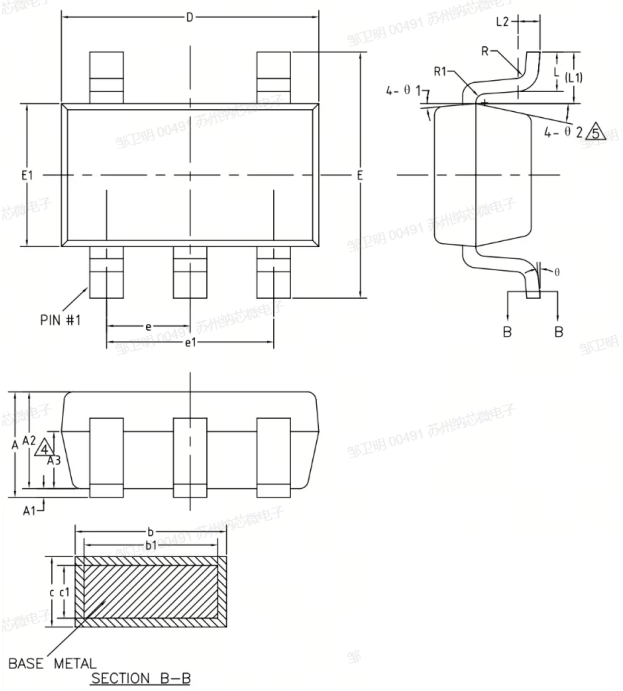


Figure 10-1 Layout Example

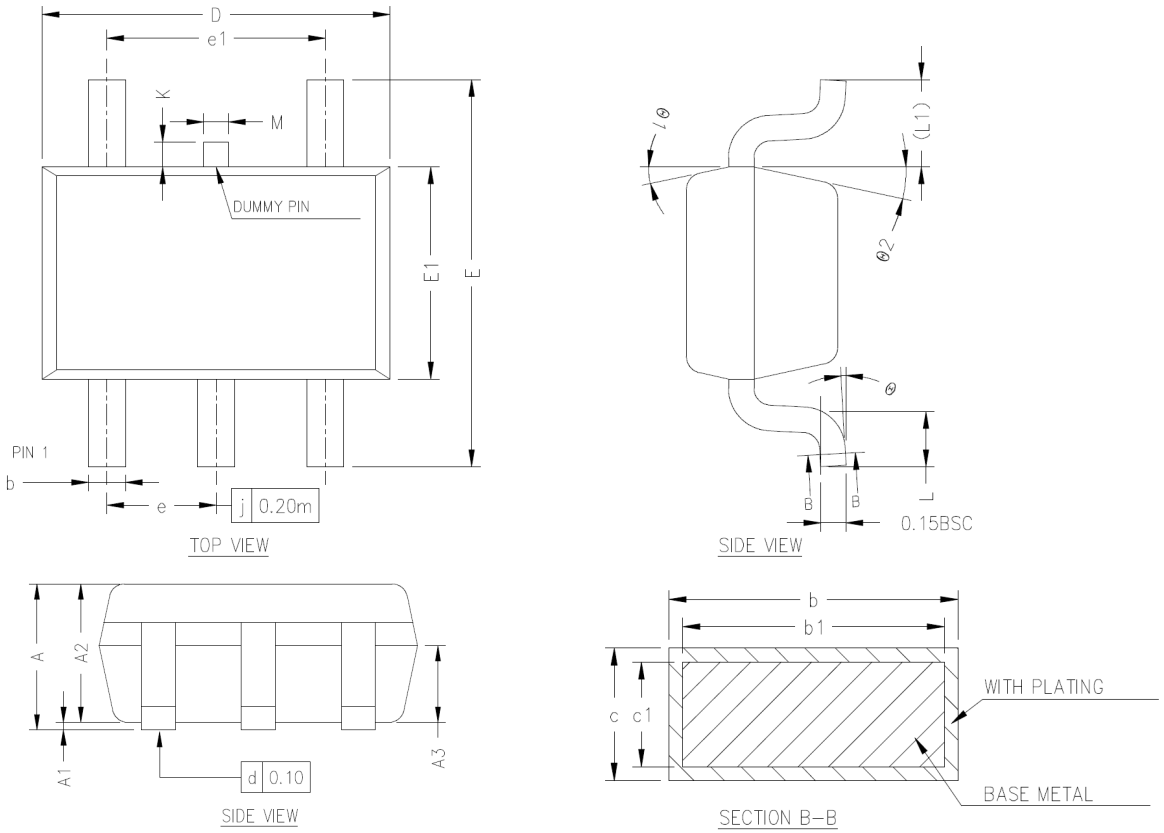
11. Package Information

SOT23-5L



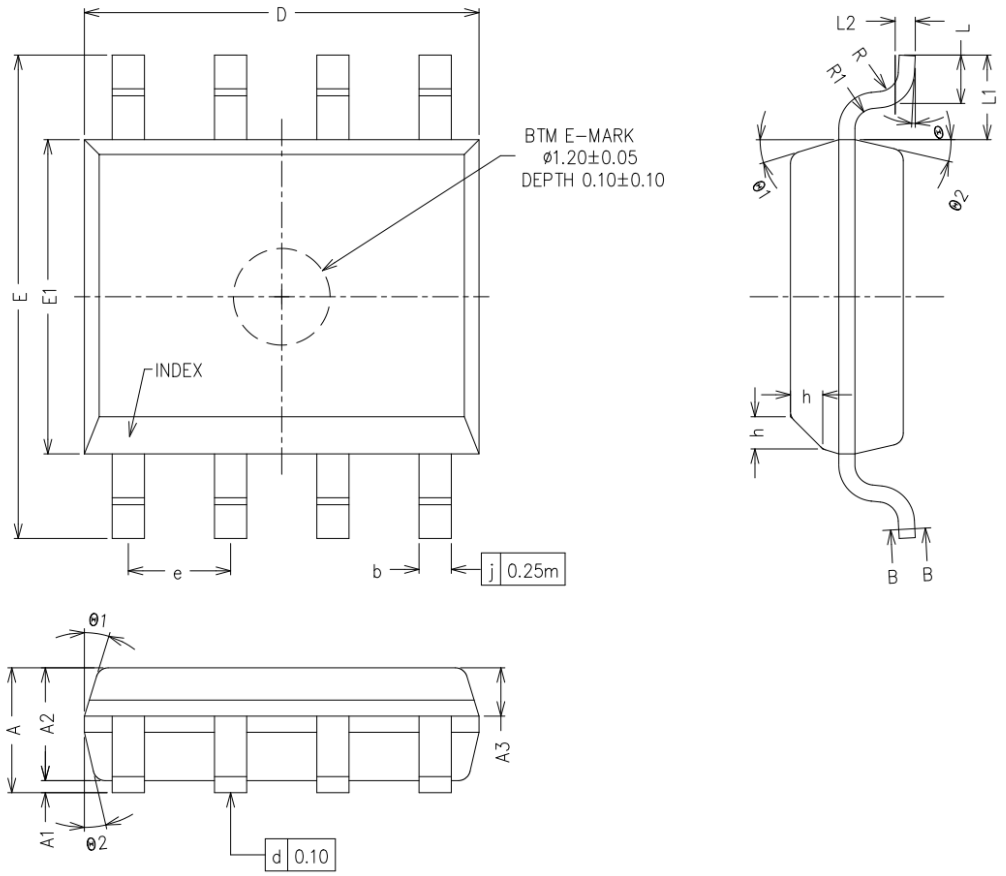
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.25	— —	0.049
A1	— —	0.15	— —	0.006
A2	1.00	1.20	0.039	0.047
A3	0.60	0.70	0.024	0.028
b	0.36	0.50	0.014	0.020
b1	0.36	0.45	0.014	0.018
c	0.14	0.20	0.006	0.008
c1	0.14	0.16	0.006	0.006
D	2.826	3.026	0.111	0.119
E	2.60	3.00	0.102	0.118
E1	1.526	1.726	0.060	0.068
e	0.90	1.00	0.035	0.039
e1	1.80	2.00	0.071	0.079
L	0.35	0.60	0.014	0.024
L1	0.59REF		0.023REF	
L2	0.25BSC		0.010BSC	
R	0.10	— —	0.004	— —
R1	0.10	0.25	0.004	0.010
θ	0°	8°	0°	8°
θ1	3°	7°	3°	7°
θ2	6°	14°	6°	14°

SC70-5



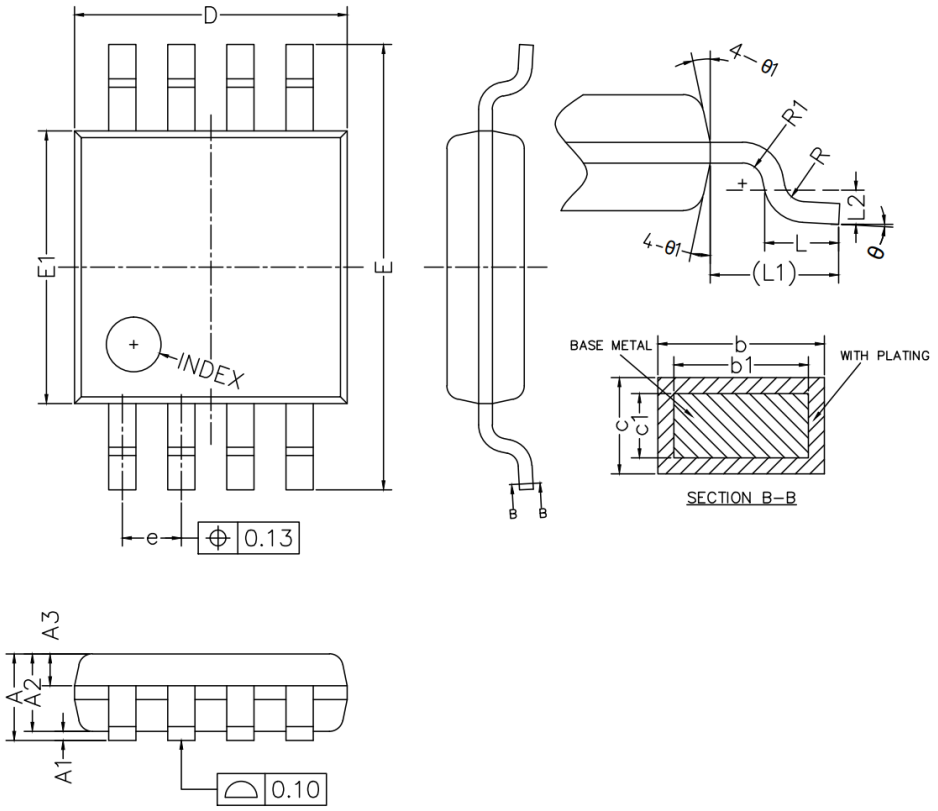
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.80	1.10	0.031	0.043
A1	0	0.10	0	0.004
A2	0.80	1.00	0.031	0.039
A3	0.40	0.60	0.016	0.024
b	0.17	0.30	0.007	0.012
b1	0.17	0.25	0.007	0.010
c	0.12	0.20	0.005	0.008
c1	0.12	0.16	0.005	0.006
D	2.02	2.12	0.080	0.083
E	2.20	2.40	0.087	0.094
E1	1.21	1.31	0.048	0.052
e	0.60	0.70	0.024	0.028
e1	1.20	1.40	0.047	0.055
L	0.26	0.46	0.010	0.018
L1	0.52REF		0.020REF	
M	0.10	0.20	0.004	0.008
K	0	0.20	0	0.008
θ	0°	8°	0°	8°
θ1	10°	14°	10°	14°
θ2	10°	14°	10°	14°

SOP8



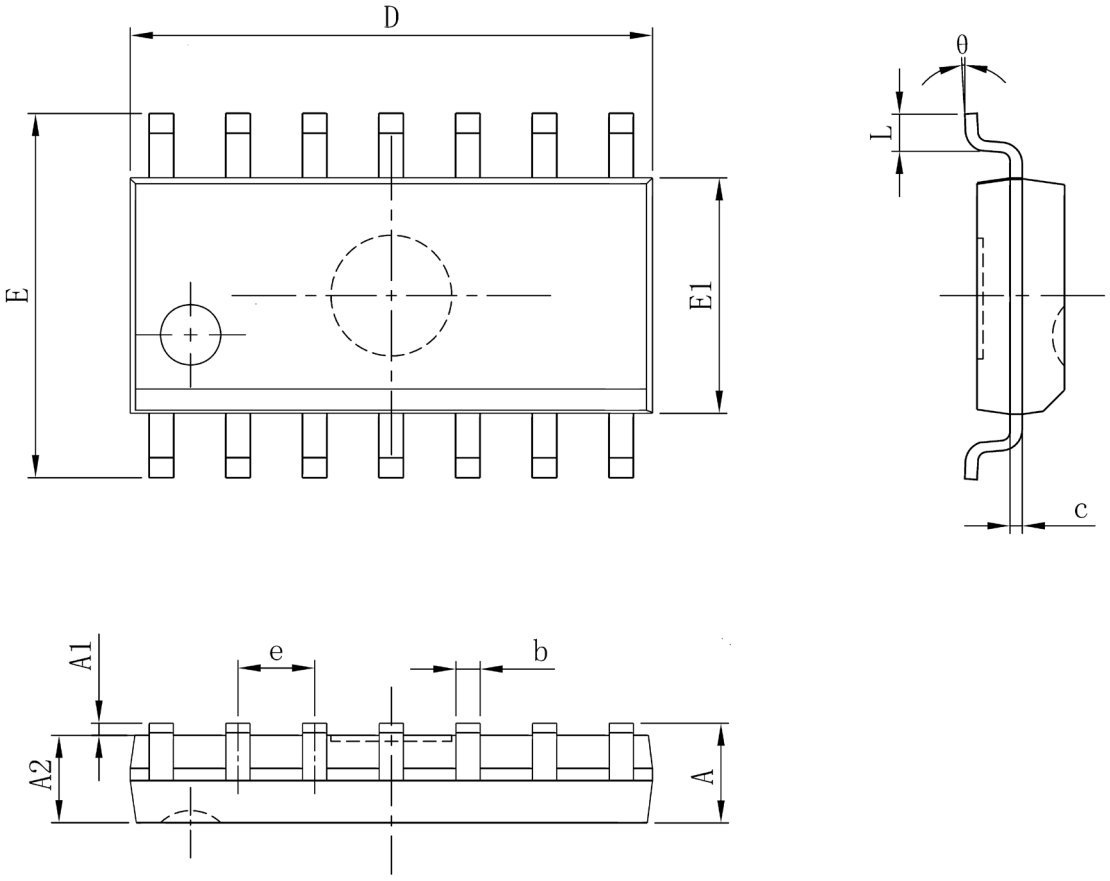
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.75	— —	0.069
A1	0.05	0.25	0.002	0.01
A2	1.30	1.50	0.051	0.059
A3	0.50	0.70	0.020	0.028
b	0.38	0.47	0.015	0.019
b1	0.37	0.40	0.015	0.016
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.15	0.157
e	1.17	1.37	0.046	0.054
L	0.45	0.80	0.018	0.031
L1	1.04REF		0.041REF	
L2	0.25BSC		0.010BSC	
R	0.07	— —	0.003	— —
R1	0.07	— —	0.003	— —
h	0.30	0.50	0.012	0.020
θ	0°	8°	0°	8°
θ1	15°	19°	15°	19°
θ2	11°	15°	11°	15°

MSOP8



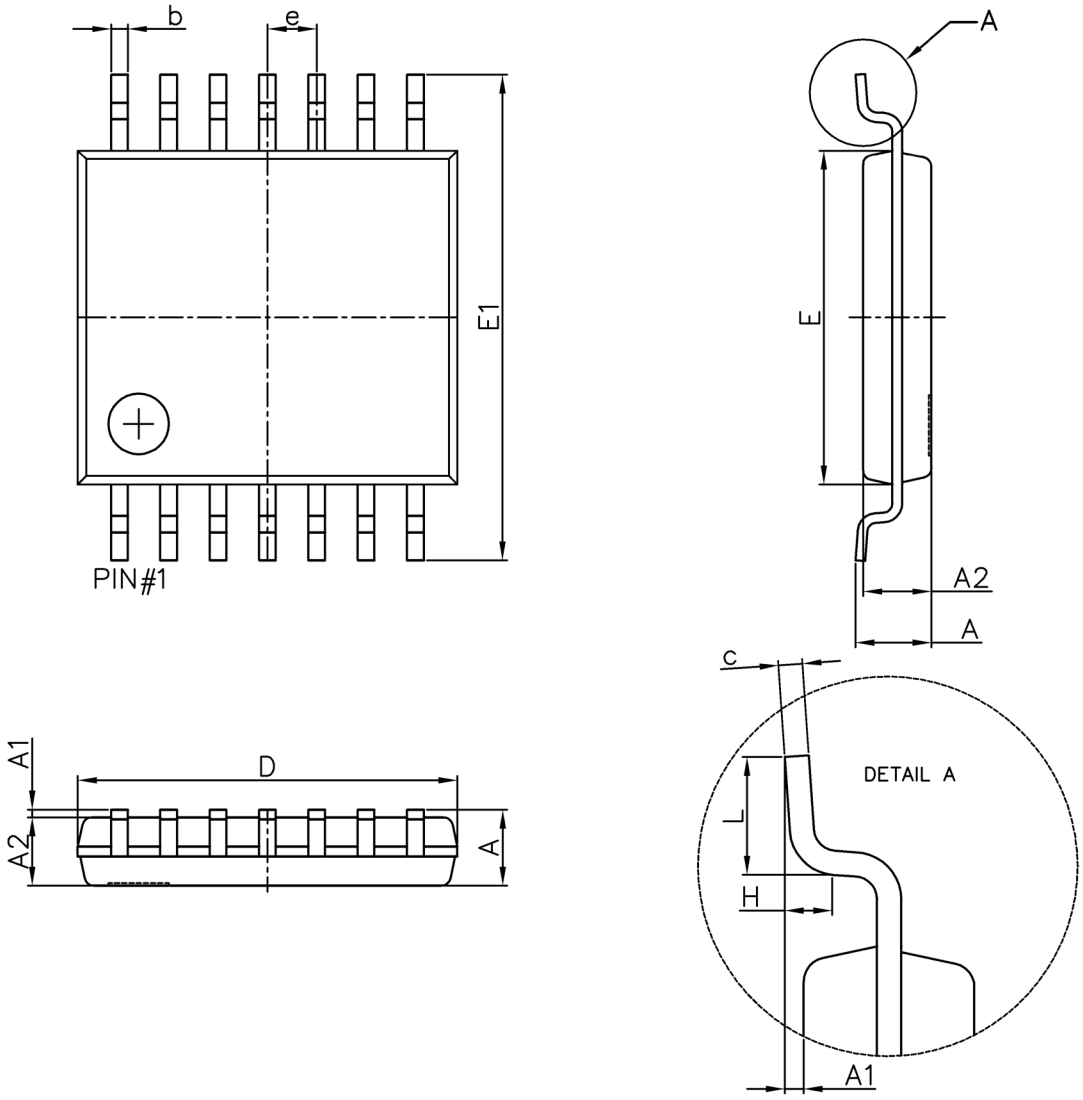
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.10	— —	0.043
A1	0.05	0.15	0.002	0.006
A2	0.75	0.95	0.030	0.037
A3	0.30	0.40	0.012	0.016
b	0.25	0.38	0.010	0.015
b1	0.24	0.33	0.009	0.013
c	0.15	0.20	0.006	0.008
c1	0.14	0.16	0.006	0.0062
D	2.90	3.10	0.114	0.122
E	4.75	5.05	0.187	0.199
E1	2.90	3.10	0.114	0.122
e	0.55	0.75	0.022	0.030
L	0.40	0.70	0.016	0.028
L1	0.95REF		0.037(BSC)	
L2	0.25BSC		0.010	
R	0.07	— —	0°	8°
R1	0.07	— —	0.003	— —
θ	0°	8°	0°	8°
θ1	9°	15°	9°	15°

SOP14



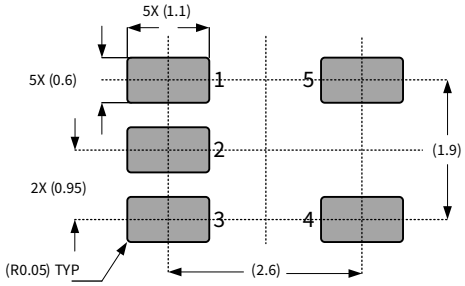
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	— —	1.75	— —	0.069
A1	0.1	0.25	0.004	0.01
A2	1.25	— —	0.049	— —
b	0.31	0.51	0.012	0.02
c	0.1	0.25	0.004	0.01
D	8.45	8.85	0.333	0.348
E	5.8	6.2	0.228	0.244
E1	3.8	4	0.15	0.157
e	1.270(BSC)		0.050(BSC)	
L	0.4	0.016	0.016	0.05
θ	0°	0°	0°	8°

TSSOP14

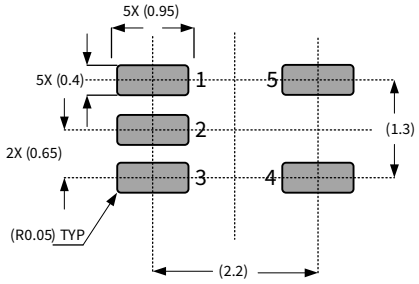


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
D	4.9	5.1	0.193	0.201
E	4.3	4.5	0.169	0.177
b	0.19	0.3	0.007	0.012
c	0.09	0.2	0.004	0.008
E1	6.25	6.55	0.246	0.258
A	—	1.2	—	0.047
A2	0.8	1	0.031	0.039
A1	0.05	0.15	0.002	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.5	0.7	0.02	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

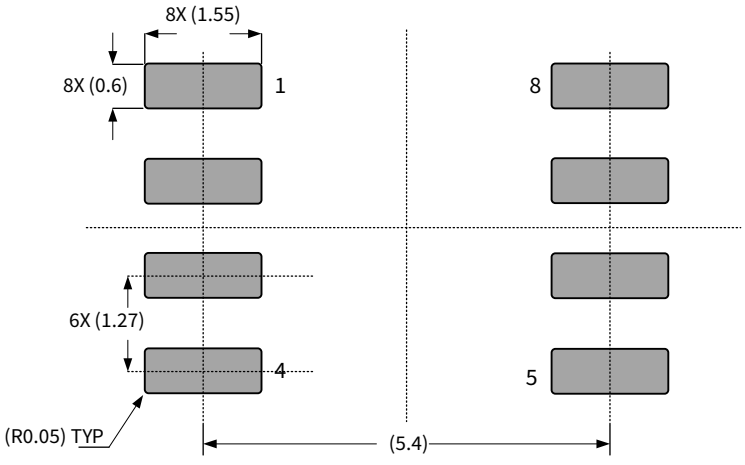
Example of Solder Pads Dimensions



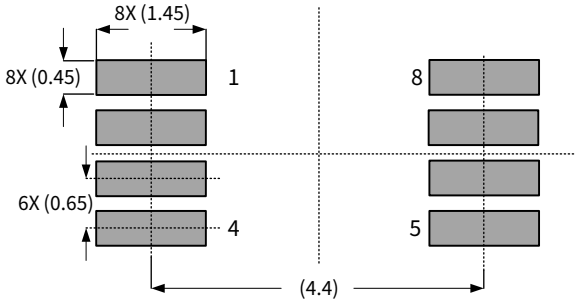
SOT23-5L



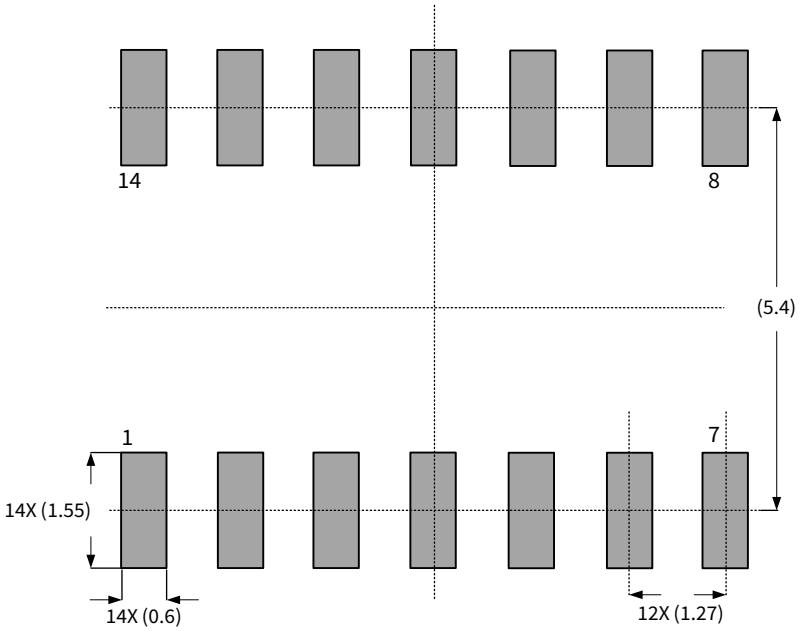
SC70-5



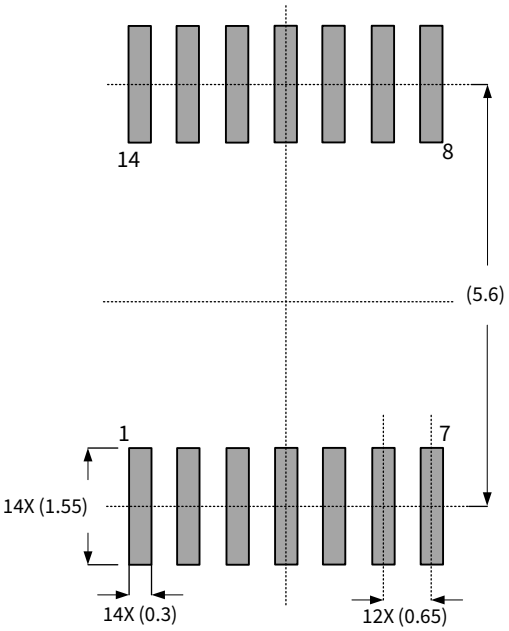
SOP8



MSOP8



SOP14



TSSOP14

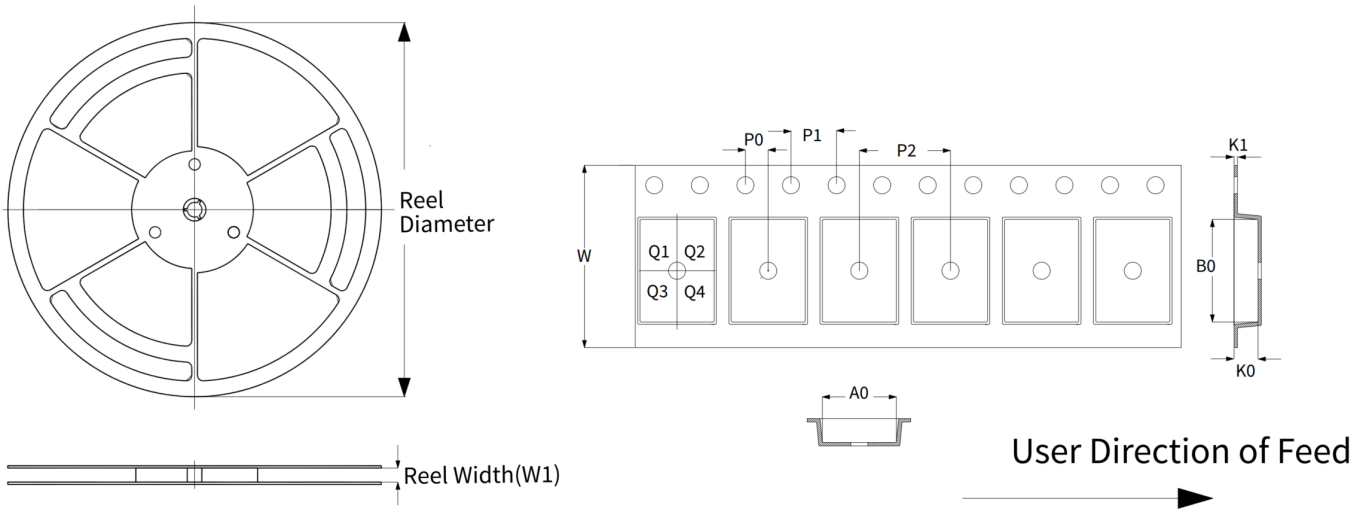
Note:

1. Unit: mm.

12. Order Information

Part Number	*Package*	*MSL Level*	*Op Temp (°C)*	*SPQ*
NSOPA8011-Q1STAR	SOT23-5L	1	-40~+125	3000
NSOPA8011-Q1SCAR	SC70-5	1	-40~+125	3000
NSOPA8012-Q1SPR	SOP8	1	-40~+125	2500
NSOPA8012-Q1MSR	MSOP8	1	-40~+125	2500
NSOPA8014-Q1SPKR	SOP14	1	-40~+125	2500
NSOPA8014-Q1TSKR	TSSOP14	1	-40~+125	4000
Note: All packages are ROHS compliant with peak reflow temperature of 260°C according to the JEDEC industry standard classifications and peak solder temperature.				

13.Tape and Reel Information



Device	Reel Diameter	Reel Width(W1)	W	A0	B0	P0	P1	P2	K0	K1	PIN1 Quadrant
NSOPA8011-Q1STAR	178	8.4	8.0	3.3	3.2	2.0	4.0	4.0	1.4	0.23	Q3
NSOPA8011-Q1SCAR	178	8.4	8.0	2.4	2.5	2.0	4.0	4.0	1.2	0.25	Q3
NSOPA8012-Q1SPR	330	12.4	12.0	6.6	5.5	2.0	4.0	8.0	2.1	0.3	Q1
NSOPA8012-Q1MSR	330	12.4	12.0	5.25	3.35	2.0	4.0	8.0	1.25	0.3	Q1
NSOPA8014-Q1SPKR	330	16.4	16.0	6.60	9.3	2.0	4.0	8.0	2.1	0.3	Q1
NSOPA8014-Q1TSKR	330	16.4	12.0	6.85	5.45	2.0	4.0	8.0	1.6	0.35	Q1

Note:

2. All dimensions are nominal.
3. The picture is only for reference. Please make the object as the standard.
4. Unit: mm.

14.Revision History

Revision	Description	Date
V1.0	Initial version	2025/01

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